# Large current modulation ratio up to 130% in a GaMnAs-based all-solid-state vertical spin metal-oxide-semiconductor field-effect transistor

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A spin metal-oxide-semiconductor field-effect transistor (spin MOSFET) is a promising candidate as a fundamental building block in next-generation electronic devices [1,2]. Recently, a *vertical* spin MOSFET, in which a current flows perpendicular to the film plane and is controlled by a gate electric field from the side surface of a mesa, has been demonstrated [3] and it exhibited much larger magnetoresistance (MR) ratios (60%) than *lateral* spin MOSFETs (less than 1% [4-6]). However, in the previous study on the vertical spin MOSFET [3], the current modulation by the gate voltage was quite small (0.5%). H. Terada *et al* reported a current modulation of ~20% in a vertical spin electric double-layer transistor [7], with ionic liquid as a gate capacitor, which is not compatible with today's electronics. Thus, all-solid-state spin MOSFETs having a large current modulation by the gate voltage are strongly required. In this study, we have fabricated an all-solid-state GaMnAs-based vertical spin MOSFET and successfully obtained the spin-valve effect as well as a large current modulation ratio up to +130% (-17%) by applying a negative (positive) gate voltage in the same device.

We grew GaMnAs-based heterostructures composed of, from the top to the bottom, $Ga_{0.94}Mn_{0.06}As$ (10 nm) / GaAs (10 nm) / $Ga_{0.94}Mn_{0.06}As$ (3.2 nm) / GaAs:Be (50 nm, hole concentration $p = 5\times10^{18}$ $cm^{-3}$) on a $p^+$-GaAs (001) substrate by low-temperature molecular beam epitaxy. After the growth, we fabricated elongated shaped mesas with a size of 500 nm × 50 μm and the comb-shaped drain electrodes connected to the top of the twenty mesas, as shown in Fig. 1(a). We deposited a 40-nm-thick $HfO_2$ layer using atomic layer deposition. We measured the drain-source current $I_{DS}$ under various drain-source voltages $V_{DS}$, applying an in-plane magnetic field $\mu_0 H$ and a gate voltage $V_{GS}$. All data were taken at 3.8 K. Figure 1(b) shows $I_{DS}$ as a function of $V_{DS}$ under various $V_{GS}$. This result clearly shows that $I_{DS}$ was successfully controlled by $V_{GS}$ and that the current modulation ratio by $V_{GS}$ amounted to +130% (-18%) at $V_{DS}$ = ~74 mV when $V_{GS}$ = -20 V (20 V), where the current modulation ratio by $V_{GS}$ is defined by $[I_{DS}(V_{GS}) / I_{DS}(V_{GS} = 0) - 1] \times 100\%$. This value (*i.e.* +130%) is 200 times larger than that obtained in the vertical spin MOSFET [3] and 6.5 times larger than that in the vertical spin electric double-layer transistor [7]. Furthermore, we found that the MR ratio tends to increase from 6.9% to 8.6% with decreasing $V_{GS}$ from 10 V to -10 V. In the presentation, we discuss the origins of these phenomena.

This work was partly supported by Grants-in-Aid for Scientific Research and Spintronics Research Network of Japan. T. Kanaki was supported by JSPS through the program for Leading Graduate Schools (MERIT). T. Kanaki thanks the JSPS Research Fellowship Program for Young Scientists.

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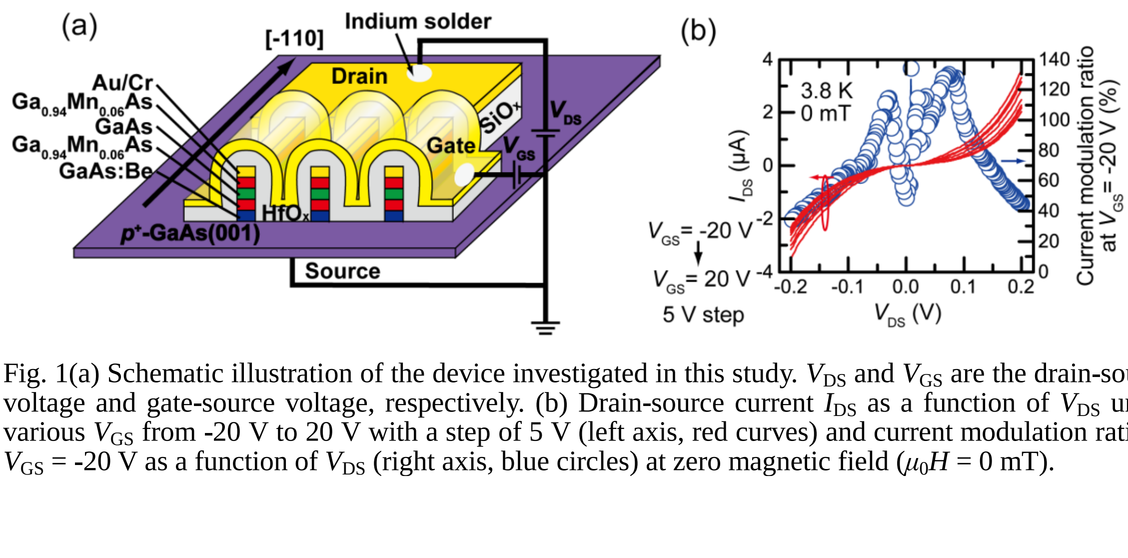


Fig. 1(a) Schematic illustration of the device investigated in this study. $V_{DS}$ and $V_{GS}$ are the drain-source voltage and gate-source voltage, respectively. (b) Drain-source current $I_{DS}$ as a function of $V_{DS}$ under various $V_{GS}$ from -20 V to 20 V with a step of 5 V (left axis, red curves) and current modulation ratio at $V_{GS}$ = -20 V as a function of $V_{DS}$ (right axis, blue circles) at zero magnetic field ($\mu_0 H$ = 0 mT).