Development of 72K Ultra-High-Resolution SLMoG system for high-capacity digital holography image

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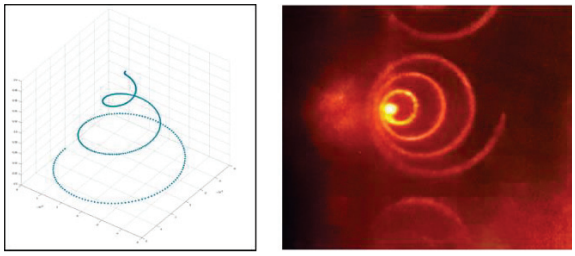
ABSTRACT

We present ultra-high-resolution digital holography operation system supporting 72K x 3.2K spatial-light-modulator on glass (SLMoG) panel which is composed of the state-of-the-art 1μm-pitch pixel. To control the high-capacity digital holography image, we have developed 40 Gbps optical transmit (Tx) / receive (Rx) and high-speed data handling system. Furthermore, we designed 6K channel of source driver IC with 1:2 demultiplexer (DeMux) control signal to operate 72K column line by using multi-MIPI interface.

1. INTRODUCTION

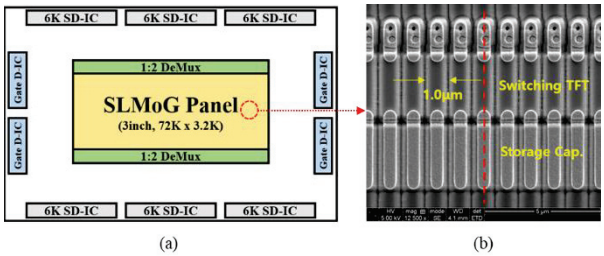
Recent digital holography research is focused on wider viewing angle, depth perception and reality. Best of all, implementation of small pixel pitch is inevitable for realistic digital hologram image because narrow pixel pitch can provide wider viewing angle of holographic image. In our previous work, we developed spatial-light-modulator-on-glass (SLMoG) which composed of 3um pitch pixel array [1] and successfully showed reconstructed 3D holography image with 10.17 viewing angle (see Fig. 1(b)).



(a) (b)

Fig. 1 Holographic Image reconstruction results of previously developed SLMoG (a) input CGH image and (b) holography image using point-like LED light

To achieve more wider viewing angle, we taken a step forward to develop 1um pitch pixel structure for viewing angle of 30 degrees. Earlier reported ultra-fine-pitch (1μm) pixel structure [2] is considered as a good candidate for high resolution holographic panel fabrication. As well as the fabrication of high-resolution panel, meanwhile, high-speed and wide-bandwidth handling technology for high-capacity computer generated holographic (CGH) image should be simultaneously developed. Conventional display image processing systems for SUHD (8K) resolution home TV and PC monitor cannot offer sufficient performance for ultra-high resolution SLM having 1um pixel pitch. We developed 40 Gbps optical transmit (Tx) / receive (Rx) system using Xilinx Aurora 64B/66B interface [3], for the bandwidth requirements of 72K [H] x 3.2K [V] resolution with 4bit grayscale, which provide video streaming option for point-to-point connectivity. In this SLMoG system, an application processor (AP) controls the received and stored CGH images with the 4 embedded high-speed storages (M.2 SSD, RAID-0). In Fig. 2(a), SLMoG panel is composed of 6 source driver ICs, 4 gate driver IC, integrated 1:2 DeMux circuit and 1μm-pitch pixel array. To operate 72K column line of the proposed SLMoG panel, we developed 6K channel of source driver IC based on the Mobile Industry Processor Interface (MIPI) DSI2 and 1:2 demultiplexer (DeMux) control circuit was used for 72K x 3.2K resolution. For the super-high bitrate multi-MIPI data control, we adopt a Xilinx ultrascale+ chipset as a timing controller (TCON).



(a) (b)

Fig. 2 Block diagram of the proposed (a) SLMoG panel and (b) SEM microscope image of 1μm VST pixel array

2. EXPERIMENTAL

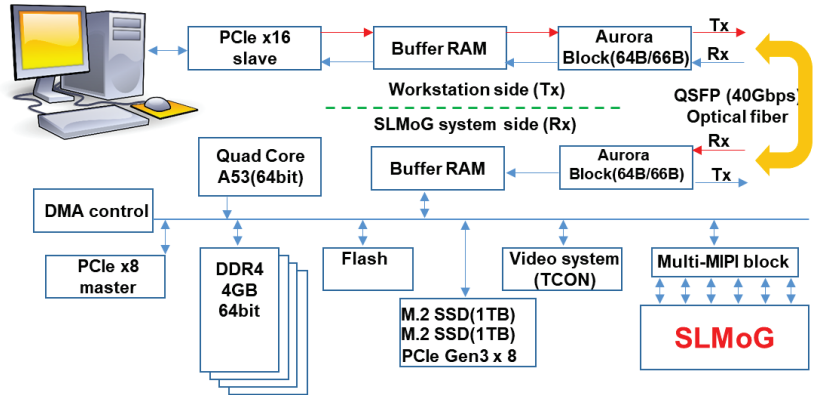


Fig. 3 Entire data flowchart for real-time data streaming and SLMoG operation system

Four key technologies are embedded on our SLMoG system. First is 1um pixel array (see Fig. 2(b)) which is placed to center area of the panel. The resolution of this array is 72K x 3.2K (3inch diagonal) and its pixel has novel transistor structure called vertically stacked TFT (VST) [2]. We fabricated 1um VST pixel structure into very narrow area by stacking transistor on data line and reflector. Second, external driver ICs are used to operate ultra-high-resolution pixel array. Especially, we used newly developed exclusive 6K output channel source driver IC for SLMoG panel driving. Third, 1:2 demultiplexer (DeMux) which multiplies 1 data line to 2 data line using timing separation method during 1 scan line time. With the 1:2 DeMux and 6 source driver ICs, 72K resolution can be achievable.

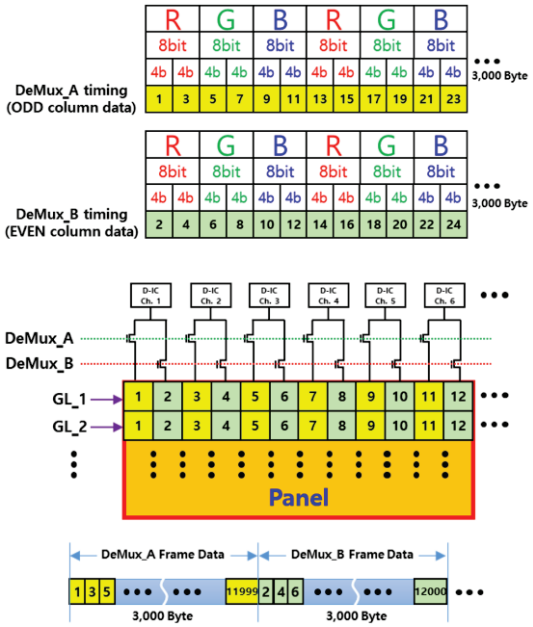


Fig. 4 Image input and output mechanism for 4bit grayscale 72K x 3.2K SLMoG panel

Final key technology is handling method for high-capacity digital holography image. Because of the large sized holography images for example uncompressed bitmap format computer generated holography (CGH), it is difficult to commercialize real-time hologram broadcasting.

For ultra-high bit-rate data transmission and data processing, we used large-capacity data handling workstation and real-time data transfer system (see Fig. 3). The bandwidth of Aurora (64B/66B) protocol with QSFP meets the target bit-rate for proposed SLMoG panel. As the required bandwidth (28 Gbps @ 24 Hz) of proposed 72K x 3.2K resolution SLMoG, image data are stored 2 pixels into 8 bits RGB data respectively. The transferred data from the QSFP ports at the data streaming workstation is stored in ODD & EVEN column line data buffers and each data get across to the pixel array synchronized with DeMux_A and DeMux_B clock signal. In Fig. 5, we designed new source driver IC based on the Mobile Industry Processor Interface (MIPI) DSI2 with D-PHY, and it supports 1:2 DeMux control signal. For test purpose, driver IC contains test option pins such as video test, additional digital analog converter (DAC) and output channel.

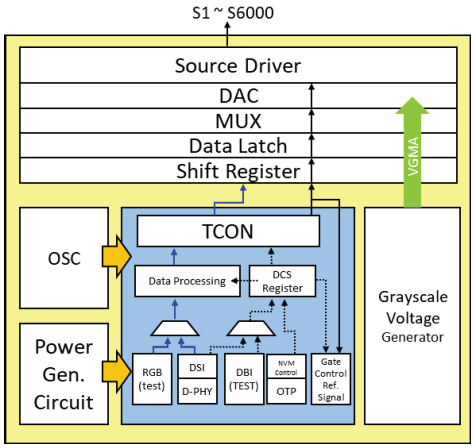


Fig. 5 System block diagram of designed 6K channel output source driver IC

3. RESULTS AND DISCUSSION

For High speed data transmission, the timing simulation is performed by using vivado logic simulator for securing MIPI D-PHY core IP. Fig. 6 shows stable timing simulation results of 1 GHz / 1 Lane. Because of the super-high bitrate multi-MIPI data, we used a Xilinx ultrascale+ chipset as a timing TCON.

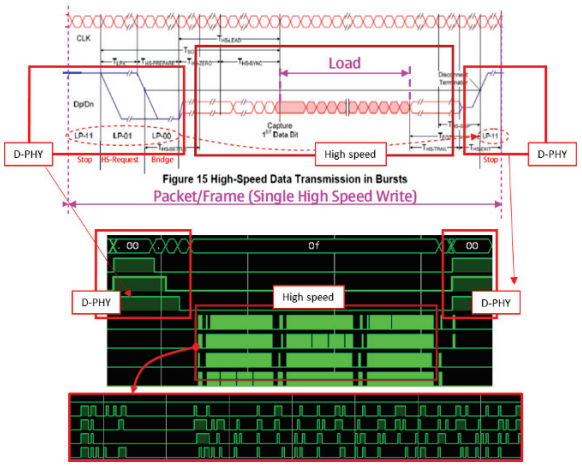


Fig. 6 RTL Simulation results of MIPI D-PHY core IP

The processing speed of the data storage devices in the streaming workstation are also important. Because slow data storage degrades the performance of the whole SLMoG system, we set up high-speed M.2 solid state drive (SSD) with RAID-0. Developed system shows high performance up to 80 Gbps (Read) and 60 Gbps (Write) processing 154 MB data on the 4.1 TB block devices. This is sufficient data storage performance to ensure real-time data streaming. (see Fig. 7)

Fig. 7 Data handling performance of the real-time data streaming workstation

Fig. 8. shows optical data transmission performance by using Aurora 64B/66B with QSFP. The proposed system is achieved 40 Gbps transfer speed when we set up loop-back test board on the Xilinx Zynq ultra-scale+ MPSoC for optical transmission and receive test. Assuming 70% resource rate of the PCI-express bus system, estimated transmission speed will be about 28.8 Gbps, and this performance is sufficient for high-capacity digital holography images processing for the proposed 72K x 3.2K SLMoG system.

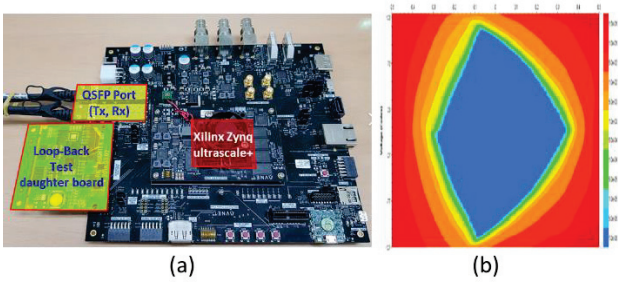


Fig. 8 (a) Optical data transmission performance test setup (Zynq ultrascale+ MPSoC) and (b) Eye diagram test result

4. CONCLUSIONS

We developed 72K x 3.2K resolution SLMoG system for high-capacity digital holography images. The proposed SLMoG system architecture will be key cornerstone for early commercialization of digital holography and other ultra-high resolution display application.

Acknowledgments

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5. REFERENCES

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