High Mobility Metal-Oxide Devices for Display SoP and 3D Brain-Mimicking IC

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ABSTRACT

Owing to fast technology evolution, the n-type SnO_2 thin-film transistor (TFT) can reach high mobility of 238 cm^2/Vs and p-type SnO TFT has high hole mobility of 7.6 cm^2/Vs. These high mobility complementary TFTs is the enabling technology for display system-on-panel and the ultra-fast three-dimensional brain-mimicking IC.

1 INTRODUCTION

Traditionally, the high performance integrated circuit (IC) was made on single-crystal Si, GaAs and InP wafers due to their high mobility in single-crystal substrate. However, one major issue of high-performance ICs is the nearly limited operation speed that only improves by ~2 times for the past two decades, while the devices were down-scaling from 90 nm to 7 nm. To address the operation speed and power consumption issues, we pioneered the three-dimensional (3D) IC since 2004 [1]. The 3D IC can largely increase the operation speed by an order of magnitude due to the greatly decreased parasitic backend capacitance ($C_{parasitic}$). Besides, the switching dynamic power consumption of $C_{parasitic}V_{DD}^2f/2$ is also largely improved due to the lowered $C_{parasitic}$, where V_{DD} and f are the power supply voltage and operation frequency respectively [2]. Although such 3D IC has been implemented in Apple's microprocessor by using package technology, the very limited vertically connecting vias are the fundamental drawback for speed and power improvement rather than the major merit of decreased package size. To realize the monolithic 3D IC to mimic the brain architecture, we initiated the high-mobility n-type SnO_2 [3]-[5], passivated-ZnO [6], and p-type SnO TFTs [7] that were fabricated on amorphous SiO_2 without using the crystalline substrate. The amorphous SiO_2 is the standard material for IC's backend inter-metal dielectric (IMD), which is also the glass substrate for display panel. Therefore, such high-mobility complementary TFTs (C-TFTs) are the enabling technology for embedded system-on-panel (SoP) of display.

2 EXPERIMENT

The Si wafers were used as the carriers for processing. After the standard RCA clean, a thick SiO_2 was formed on Si wafer, which is the common material for IMD and display panel. A 60 nm TaN was deposited on SiO_2 through DC sputtering as the bottom gate.

For nTFT, three different kinds of the high-κ gate stacks were made by physical vapor deposition (PVD) to examine the device performance: $SiO_2/Al_2O_3/HfO_2$, $Al_2O_3/Al_2O_3/HfO_2$ and $HfO_2/Al_2O_3/HfO_2$. The dielectric layers were annealed at 400°C after deposition. Then, an ultra-thin 5 nm SnO_2 channel layer was deposited by reactive sputtering at a DC power of 50 W. After deposition, the devices were annealed at 400°C in an oxygen ambient. Finally, a 300 nm thick Aluminum was deposited as the source/drain contact.

For pTFT, the bottom SiO_2 and TaN gate electrode were the same as nTFT. Then a single gate dielectric of 40-nm-thick high-κ HfO_2 was deposited through PVD and annealed at 400 °C. After that, a 12 nm SnO was deposited by sputtering in an Ar/O_2 mixture from a Sn target, under a DC power of 50 W. The SnO channel layer was annealed at 200°C in a N_2 ambient. Finally, the Ni was deposited to form the source-drain electrodes. For both pTFT and nTFT, the channel length and width were 50 μm and 500 μm, respectively.

3 RESULTS AND DISCUSSION

Figure 1 displays the schematic diagram of the monolithic 3D IC structure. To form the electronic neurons, both the logic C-TFTs and embedded memory devices [8]-[11] are needed. One promising embedded memory is the resistive random access memory (RRAM) that has simple structure and can be easily integrated into IC's backend like C-TFTs. Figure 2 shows the dynamic power consumption versus operation frequency, which was obtained from Electro-Magnetic calculation of 1-cm long parallel backend interconnect lines. At the same frequency, the power consumption can be significantly improved by changing the planar 2D into 1-folding and 2-folding monolithic 3D structure, where the interconnect distance is largely decreased. In addition, under a constant power computation, the operation speed can also be increased from 2D into 3D structure. Such improvement in both dynamic power consumption and operation frequency is due to the decreased $C_{parasitic}$ by 3D integration. Therefore, the monolithic 3D structure is the key technology to realize the low-power brain-mimicking IC [1]-[2].

Figure 3 shows the transistors' drain current-gate voltage (I_{DS}-V_{GS}) characteristics of bottom-metal-gate/ high-κ SnO_2 nTFTs. Both the drive currents and the threshold voltage depend strongly on the gate-stack design. The high-κ gate stack is also the essential

technology to hugely lower the operation voltage and power. Figure 4 plots the field-effect mobility (μ_{FE}) versus V_G characteristics of these transistors. The mobility increases monotonically from using interfacial HfO_2, Al_2O_3, to SiO_2 layers. Such improvement is due to the excellent material property and relatively low interface dipole of SiO_2. Therefore, the proper device structure design is crucial to reach high mobility. A high μ_{FE} of 238 cm^2/Vs is obtained using the optimized high-κ gate stacks with the SiO_2 interfacial layer. One important merit of SnO_2 transistor is its wide energy bandgap of 3.7 eV that is much larger than the 1.1 eV of Si. Thus, the SnO_2 TFT can be operated even more than 200°C [4]. Besides, the measured μ_{FE} is higher than SiC and GaN nMOSFET [12], which is due to the small effective mass of SnO_2 material [3].

The pTFT is essential to form the ultra-low DC power C-TFTs. Among known p-type materials, the SnO has the lowest effective mass from 1st principle quantum-mechanical calculation that is due to the single hole band without heavy hole band [7]. Figure 5 shows the measured I_D-V_G characteristics of bottom-metal-gate/HfO_2 SnO pTFT. Here a single high-κ layer is used because the scattering mechanism of hole mobility is due to channel SnO material rather than the interfacial layer. A sharp turn on subthreshold slope of 140 mV/dec is obtained. Figure 6 depicts the μ_{FE}-V_G characteristics derived from the I_D-V_G characteristics. A relatively high hole mobility of 7.6 cm^2/Vs was reached, which is one of the highest hole μ_{FE} reported to date. Although this hole mobility value is still inferior to SiO_2/Si pMOSFET, the main delay in advanced microprocessor is from the IC's interconnects rather than from the transistors. Besides, the major merit in the brain is the 3D parallel operation that can be mimicked by such monolithic 3D structure made on IC's backend. Such high performance C-TFTs are also the enabling technology to realize display SoP on glass and decrease the pixel size.

4 CONCLUSION

The monolithic 3D integration is the enabling technology to improve both the operation frequency and dynamic power consumption of advanced microprocessor. The originality and novelty of this work are the design of high-κ gate stack and engineering the high-mobility SnO_2 and SnO channel materials for respective nTFT and pTFT, which are crucially related to the mobility of metal-oxide transistors. The high mobility metal-oxide C-TFTs made on amorphous SiO_2 are the essential technology for both 3D brain-mimicking IC and display SoP.

REFERENCES

[1] D. S. Yu, Albert Chin, C. C. Laio, C. F. Lee, C. F. Cheng, W. J. Chen, C. Zhu, M.-F. Li, S. P. McAlister, and D. L. Kwong, "3D GOI CMOSFETs with Novel IrO_2(Hf) dual gates and high-κ dielectric on 1P6M-0.18μm-CMOS," *IEEE IEDM Tech. Dig.*, pp. 181-184 (2004).

[2] Albert Chin and Y. D. Chen, "Technologies Toward Three-dimensional brain-mimicking IC architecture," *IEEE Electron Devices Tech. Manufacturing Conf.* (*EDTM*) *Tech. Dig.,* pp. 472-474 (2019).

[3] C. W. Shih, Albert Chin, C. F. Lu and S. H. Yi, "Extremely high mobility ultra-thin metal-oxide with ns2np2 configuration," *IEEE IEDM Tech. Dig*., pp. 145-148 (2015).

[4] C. W. Shih, and A. Chin, "New Material Transistor with Record high field-effect mobility among wide-bandgap semiconductors," *ACS Appl. Mater. Interfaces*, vol. 8, pp. 19187-19191 (2016).

[5] C. W. Shih, A. Chin, C. F. Lu, and W. F. Su, "Remarkably high mobility ultra-thin-film metal-oxide transistor with strongly overlapped orbitals," *Sci. Reports,* vol. 6, p. 19023 (2016).

[6] C. W. Shih, A. Chin, C. F. Lu, and W. F. Su, "Remarkably high mobility thin-film transistor on flexible substrate by novel passivation material," *Sci. Reports*, vol. 7, p. 1147 (2017).

[7] C. W. Shih, A. Chin, C. F. Lu, and W. F. Su, "Remarkably high hole mobility metal-oxide thin-film transistors," *Sci. Reports*, vol. 8, p. 889 (2018).

[8] B. Gao, H. Wu, W. Wu, X. Wang, P. Yao, Y. Xi, W. Zhang, N. Deng, P. Huang, X. Liu, J. Kang, H. Chen, S. Yu, and H. Qian, "Modeling disorder effect of the oxygen vacancy distribution in filamentary analog RRAM for neuromorphic computing," *IEEE IEDM Tech. Dig.*, pp. 441-444 (2017).

[9] P. Yao, H. Wu, B. Gao, S. B. Eryilmaz, X. Huang, W. Zhang, Q. Zhang, N. Deng, L. Shi, H.-S. P. Wong, and H. Qian, "Face classification using electronic synapses," *Nature Commun*., vol. 8, p. 15199 (2017).

[10] M. Zackriya V, H. M. Kittur, and Albert Chin, "A novel read scheme for large size one-resistor resistive random access memory array," *Sci. Reports*, vol. 7, p. 42375 (2017).

[11] M. Zackriya V, Albert Chin, and H. M. Kittur, "Impact of current distribution on RRAM array with high and low I_{ON}/I_{OFF} devices," *IEEE Electron Devices Technology & Manufacturing Conference (EDTM) Tech. Dig*., pp. 156-157 (2017).

[12] S. H. Yi, D. B. Ruan, S. Y. Di, X. Y. Liu, Y. H. Wu and A. Chin, "High performance metal-gate/high-κ GaN MOSFET with good reliability for both logic and power applications," *IEEE J. Electron Devices Soc.*, vol. 4, pp. 246-252 (2016).

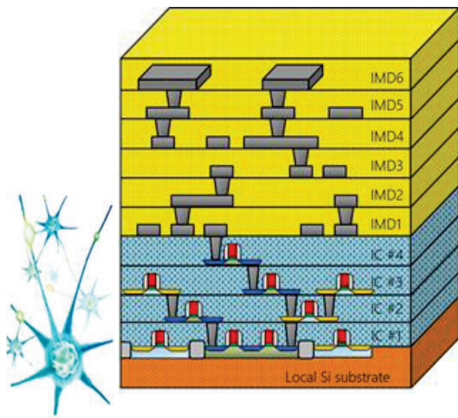

Fig. 1 The schematic diagram of 3D IC structure.

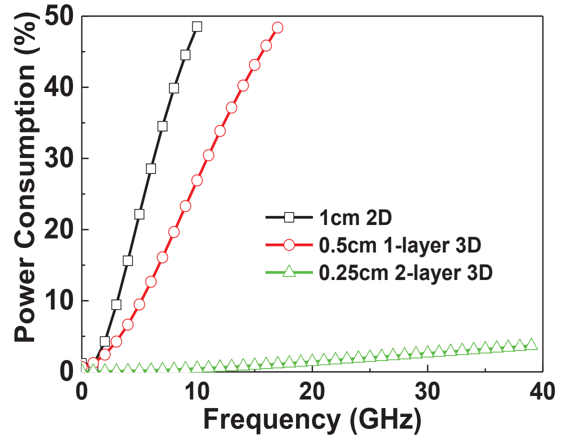

Fig. 2 The power consumption vs. operation frequency.

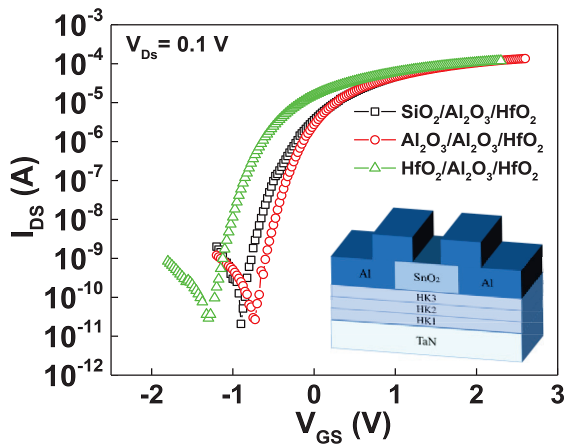

Fig. 3. The I_D-V_G characteristics of metal-gate/ high-κ SnO_2 nTFTs with different gate structure.

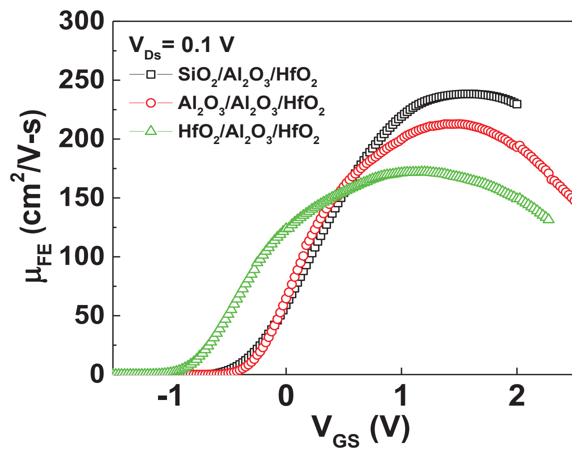

Fig. 4. The μ_{FE}-V_G characteristics of metal-gate/ high-κ SnO_2 nTFTs.

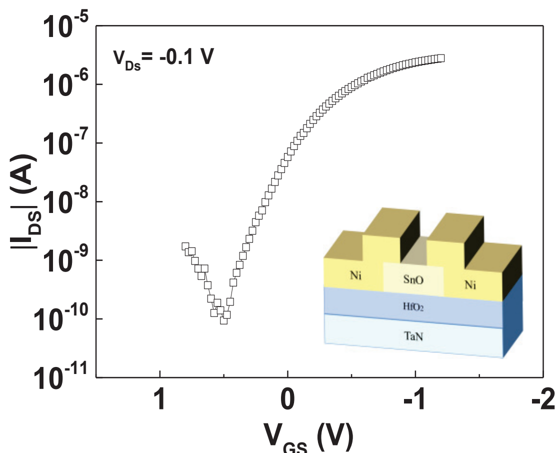

Fig. 5. The I_D-V_G characteristics of metal-gate/ high-κ SnO pTFT with inserted device structure.

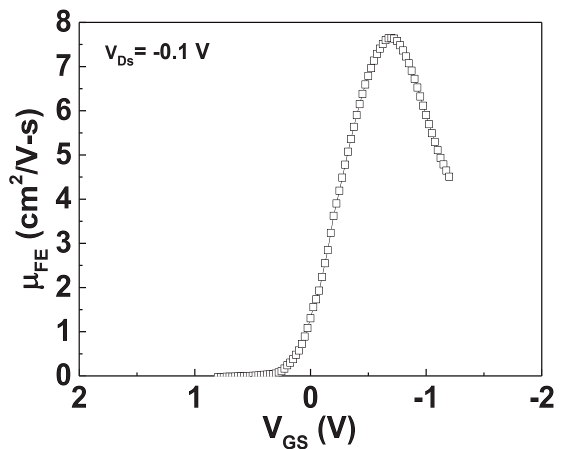

Fig. 6. The μ_{FE}-V_G characteristics of metal-gate/ high-κ SnO pTFT.