High Mobility Metal-Oxide Devices for Display SoP and 3D Brain-Mimicking IC

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ABSTRACT

Owing to fast technology evolution, the n-type SnO thin-film transistor (TFT) can reach high mobility of 238 cm^2/Vs and p-type SnO TFT has high hole mobility of 7.6 cm^2/Vs. These high mobility complementary TFTs is the enabling technology for display system-on-panel and the ultra-fast three-dimensional brain-mimicking IC.

1 INTRODUCTION

Traditionally, the high performance integrated circuit (IC) was made on single-crystal Si, GaAs and InP wafers due to their high mobility in single-crystal substrate. However, one major issue of high-performance ICs is the nearly limited operation speed that only improves by ~2 times for the past two decades, while the devices were down-scaling from 90 nm to 7 nm. To address the operation speed and power consumption issues, we pioneered the three-dimensional (3D) IC since 2004 [1]. The 3D IC can largely increase the operation speed by an order of magnitude due to the greatly decreased parasitic backend capacitance (C_{parasitic}). Besides, the switching dynamic power consumption of C_{parasitic}V^2DDf/2 is also largely improved due to the lowered C_{parasitic}, where VDD and f are the power supply voltage and operation frequency respectively [2]. Although such 3D IC has been implemented in Apple’s microprocessor by using package technique, the very limited connecting vias are the fundamental drawback for speed and power improvement rather than the major merit of decreased package size. To realize the monolithic 3D IC to mimic the brain architecture, we initiated the high-mobility n-type SnO [3]-[5], passivated-ZnO [6], and p-type SnO TFTs [7] that were fabricated on amorphous SiO2 without using the crystalline substrate. The amorphous SiO2 is the standard material for IC’s backend inter-metal dielectric (IMD), which is also the glass substrate for display panel. Therefore, such high-mobility complementary TFTs (C-TFTs) are the enabling technology for embedded system-on-panel (SoP) of display.

2 EXPERIMENT

The Si wafers were used as the carriers for processing. After the standard RCA clean, a thick SiO2 was formed on Si wafer, which is the common material for IMD and display panel. A 60 nm TaN was deposited on SiO2 through DC sputtering as the bottom gate. For nTFT, three different kinds of the high-κ gate stacks were made by physical vapor deposition (PVD) to examine the device performance: SiO2/Al2O3/HfO2, Al2O3/Al2O3/HfO2 and HfO2/Al2O3/HfO2. The dielectric layers were annealed at 400°C after deposition. Then, an ultra-thin 5 nm SnO2 channel layer was deposited by reactive sputtering at a DC power of 50 W. After deposition, the devices were annealed at 400°C in an oxygen ambient. Finally, a 300 nm thick Aluminum was deposited as the source/drain contact.

For pTFT, the bottom SiO2 and TaN gate electrode were the same as nTFT. Then a single gate dielectric of 40-nm-thick high-κ HfO2 was deposited through PVD and annealed at 400 °C. After that, a 12 nm SnO was deposited by sputtering in an Ar/O2 mixture from a Sn target, under a DC power of 50 W. The SnO channel layer was annealed at 200°C in a N2 ambient. Finally, the Ni was deposited to form the source/drain electrodes. For both pTFT and nTFT, the channel length and width were 50 μm and 500 μm, respectively.

3 RESULTS AND DISCUSSION

Figure 1 displays the schematic diagram of the monolithic 3D IC structure. To form the electronic neurons, both the logic C-TFTs and embedded memory devices [8]-[11] are needed. One promising embedded memory is the resistive random access memory (RRAM) that has simple structure and can be easily integrated into IC’s backend like C-TFTs. Figure 2 shows the dynamic power consumption versus operation frequency, which was obtained from Electro-Magnetic calculation of 1-cm long parallel backend interconnect lines. At the same frequency, the power consumption can be significantly improved by changing the planar 2D into 1-folding and 2-folding monolithic 3D structure, where the interconnect distance is largely decreased. In addition, under a constant power computation, the operation speed can also be increased from 2D into 3D structure. Such improvement in both dynamic power consumption and operation frequency is due to the decreased C_{parasitic} by 3D integration. Therefore, the monolithic 3D structure is the key technology to realize the low-power brain-mimicking IC [1][2].

Figure 3 shows the transistors’ drain current-gate voltage (I_D, V_G) characteristics of bottom-metal-gate/ high-κ SnO2 nTFTs. Both the drive currents and the threshold voltage depend strongly on the gate-stack design. The high-κ gate stack is also the essential
technology to hugely lower the operation voltage and power. Figure 4 plots the field-effect mobility ($\mu_{FE}$) versus $V_G$ characteristics of these transistors. The mobility increases monotonically from using interfacial HfO$_2$, Al$_2$O$_3$, to SiO$_2$ layers. Such improvement is due to the excellent material property and relatively low interface dipole of SiO$_2$. Therefore, the proper device structure design is crucial to reach high mobility. A high $\mu_{FE}$ of 238 cm$^2$/Vs is obtained using the optimized high-$\kappa$ gate stacks with the SiO$_2$ interfacial layer. One important merit of SnO$_2$ transistor is its wide energy bandgap of 3.7 eV that is much larger than the 1.1 eV of Si. Thus, the SnO$_2$ TFT can be operated even more than 200°C [4]. Besides, the measured $\mu_{FE}$ is higher than SiC and GaN nMOSFET [12], which is due to the small effective mass of SnO$_2$ material [3].

The pTFT is essential to form the ultra-low DC power C-TFTs. Among known p-type materials, the SnO has the lowest effective mass from 1st principle quantum-mechanical calculation that is due to the single hole band without heavy hole band [7]. Figure 5 shows the measured $I_D$-$V_G$ characteristics of bottom-metal-gate/HfO$_2$ SnO pTFT. Here a single high-$\kappa$ layer is used because the scattering mechanism of hole mobility is due to channel SnO material rather than the interfacial layer. A sharp turn on subthreshold slope of 140 mV/dec is obtained. Figure 6 depicts the $\mu_{FE}$-$V_G$ characteristics derived from the $I_D$-$V_G$ characteristics. A relatively high hole mobility of 7.6 cm$^2$/Vs was reached, which is one of the highest hole $\mu_{FE}$ reported to date. Although this hole mobility value is still inferior to SiO$_2$/Si pMOSFET, the main delay in advanced microprocessor is from the IC’s interconnects rather than from the transistors. Besides, the major merit in the brain is the 3D parallel operation that can be mimicked by such monolithic 3D structure made on IC’s backend. Such high performance C-TFTs are also the enabling technology to realize display SoP on glass and decrease the pixel size.

4 CONCLUSION

The monolithic 3D integration is the enabling technology to improve both the operation frequency and dynamic power consumption of advanced microprocessor. The originality and novelty of this work are the design of high-$\kappa$ gate stack and engineering the high-mobility SnO$_2$ and SnO channel materials for respective nTFT and pTFT, which are crucially related to the mobility of metal-oxide transistors. The high mobility metal-oxide C-TFTs made on amorphous SiO$_2$ are the essential technology for both 3D brain-mimicking IC and display SoP.

REFERENCES


Fig. 1 The schematic diagram of 3D IC structure.

Fig. 2 The power consumption vs. operation frequency.

Fig. 3. The $I_{DS}-V_{GS}$ characteristics of metal-gate/ high-$\kappa$ SnO$_2$ nTFTs with different gate structure.

Fig. 4. The $\mu_{FE}-V_{GS}$ characteristics of metal-gate/ high-$\kappa$ SnO$_2$ nTFTs.

Fig. 5. The $I_{DS}-V_{GS}$ characteristics of metal-gate/ high-$\kappa$ SnO pTFT with inserted device structure.

Fig. 6. The $\mu_{FE}-V_{GS}$ characteristics of metal-gate/ high-$\kappa$ SnO pTFT.