Top-Gate Oxide TFTs with Ion-Implanted Source/Drain Regions in Advanced LTPS Technology

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ABSTRACT

This study develops advanced LTPS TFT technology with top-gate self-aligned oxide TFTs using Generation 6 mother glass. Source and drain regions of the oxide TFTs are formed by ion implantation through a gate insulator with a gate metal mask. The optimized oxide TFTs demonstrates good short-channel performance.

1 INTRODUCTION

Oxide thin-film-transistors (TFTs) have attracted a lot of attention owing to low-temperature processing [1] and low off-state current [2]. Top-gate self-aligned (TGSA) oxide TFT technology has vigorously developed for medium- and large-sized organic light emitting diode (OLED) displays [3, 4]. This is because parasitic capacitance should be reduced to suppress power consumption by preventing the overlap between the gate electrode and the source/drain (S/D) electrode. Japan Display Inc. has also worked on its development in order to adopt advanced low-temperature polycrystalline silicon (LTPS) TFT technology for high-end liquid crystal displays (LCDs) [5, 6]. Although this technology fabricates peripheral circuits by using the complementary metal oxide semiconductor (CMOS) LTPS process, pixel TFTs are formed by using the TGSA oxide process.

Recently, to promote the high resolution of those displays, the channel length (L) of the TGSA TFTs has become shorter [7-9]. Many TGSA TFTs are fabricated by the following process flow: after patterning the gate electrode and the gate insulator (GI), S/D regions are formed by depositing adequate passivation layers. However, few studies have reported that such TFTs with short L exhibit no negative shift of threshold voltage (V_{th}) as well as low V_{th} shift (ΔV_{th}) under negative bias illumination temperature stress (NBTIS). This ΔV_{th} value should be suppressed to avoid the deterioration of display quality, especially for LCDs. On the other hand, the TGSA oxide TFTs fabricated in this study showed good characteristics even in L = 2 μm [9]. In this TFTs, ion implantation (I/I) is used to form S/D regions through GI without its patterning. Although additional process steps are needed, the TFTs fabricated thorough this process seem to be effective regarding simultaneous achievement of short L and low NBTIS ΔV_{th} value.

This paper describes advanced LTPS TFT technology, especially for the developed TGSA oxide TFT technology with ion-implanted S/D regions. Adequate process conditions were considered to improve oxide TFT characteristics, such as field-effect mobility (μ_{FE}) and sheet resistance of the n^+ oxide regions (R_{sh_n+}) at short L. Good NBTIS reliability of oxide TFTs was also confirmed by using optimized process conditions.

2 EXPERIMENT

Figure 1 provides a cross-sectional view of an advanced LTPS array. A CMOS LTPS TFT was adequately fabricated based on the conventional process on the Generation 6 mother glass substrate. After that, the TGSA oxide TFT was stacked up. A gate metal for the LTPS TFT and a light shield for the oxide TFT were formed simultaneously. Next, a dielectric interlayer which comprises silicon nitride (SiN) and silicon oxide (SiO) films was deposited via plasma-enhanced chemical vapor deposition (PECVD). An oxide layer comprising indium, gallium, zinc, and oxygen was formed via AC sputtering. An additional metal layer of titanium was patterned on the oxide layer to form S/D electrodes. This layer was formed to prevent the removal of the oxide layer during contact-hole (C/H) opening. A GI comprising a SiO film was deposited via PECVD under adequate conditions to improve the reliability of the oxide TFT. After patterning a top-gate metal electrode, n^+ oxide regions (S/D regions) of parts of the oxide layer were formed via I/I through the GI-SiO layer. In this study, boron was used as the ion species of I/I and ion energy was fixed at a selected conventional value. After that, the dielectric interlayer was deposited via PECVD for passivation of the oxide TFT. Herein, SiN (hereinafter called PAS-SiN) was deposited firstly on the oxide layer. After the deposition of the interlayer, C/H and S/D metal electrodes were formed.

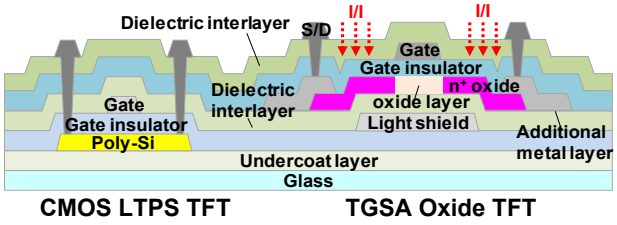
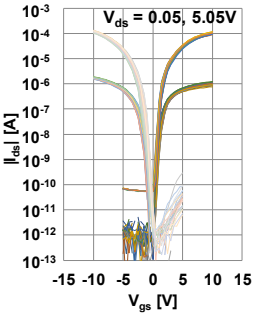


Figure 1. Schematic cross-sectional view of advanced LTPS array

3 RESULTS AND DISCUSSION

3.1 LTPS TFT performance

Figure 2 shows the current-voltage (I_{ds}-V_{gs}) transfer characteristics of LTPS TFTs with a channel width (W) of 4.5 μm and L = 3 μm, respectively. The measurements were carried out at 22 points on the Generation 6 glass substrate. Uniform TFT characteristics were observed in both N-channel (N_{ch}) and P-channel (P_{ch}) TFTs. The average values of μ_{FE} and V_{th} of TFTs are also listed below. These electrical characteristics were adequate for the application of the CMOS gate driver and the multiplexer. It was confirmed that the LTPS characteristics were unaffected by the following oxide TFT process.



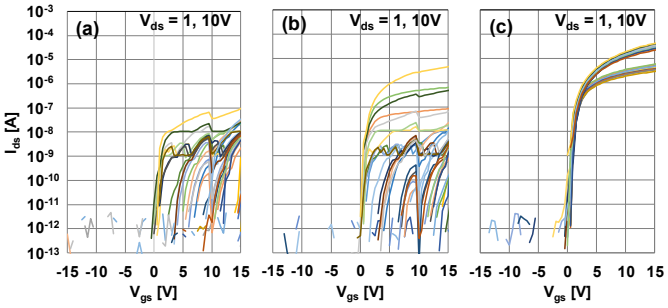
	Pch	Nch
μ_{FE} [cm²/Vs]	90	66
V_{th} [V]	-2.49	1.38

Figure 2. I_{ds}–V_{gs} transfer characteristics of LTPS TFTs with W/L = 4.5/3 μm

3.2 Consideration of TGSA oxide TFT process

In the development of TGSA oxide TFT technology, process conditions were considered first, and the results of that investigation are briefly introduced here. First, the influence of I_{ds}-V_{gs} transfer characteristics on dose amount of I/I (N_{dose}) was investigated, as shown in Fig. 3. Channel width (W) and L of TFTs were 3 and 2 μm, respectively. In the low N_{dose} value, the leakage current could not be measured because of the low current value under the measurement limit, but the observed I_{ds}-V_{gs} characteristics were poor (Fig. 3(a)). When N_{dose} increased to the middle value, except for improvement in a few I_{ds}-V_{gs} characteristics, many characteristics were still insufficient (Fig. 3(b)). On the other hand, by further increasing the N_{dose} value, higher I_{ds} with small variation and better uniformity of V_{th} were observed (Fig. 3(c)). These results indicate that the high dose of I/I is necessary to improve I_{ds}-V_{gs} transfer characteristics. However, it was noticed that despite higher N_{dose} value, μ_{FE} and R_{sh_n+} were relatively small and large, respectively. This suggests that improvement by a high dose of I/I should be incomplete.

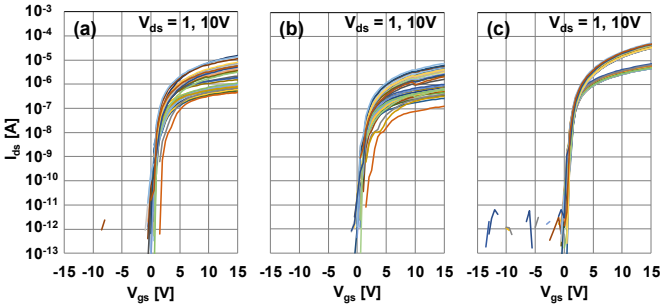
It was assumed that these results were affected by the film property of PAS-SiN because it was deposited with



	(a)	(b)	(c)
μ_{FE} [cm²/Vs]	0.04	0.11	7.3
V_{th} [V]	16.9	15.7	2.2
R_{sh_n+} [kΩ/sq]	~13000	~4700	2.2

Figure 3. I_{ds}–V_{gs} transfer characteristics of TGSA oxide TFTs (W/L = 3/2 μm) with different N_{dode} values of (a) low, (b) middle, and (c) high. The average values of electrical characteristics of those TFTs were listed below. PAS-SiN was deposited under low-hydrogen-content condition.

low hydrogen content. Further investigation of I_{ds}-V_{gs} transfer characteristics was carried out by applying PAS-SiN with higher hydrogen content, as shown in Fig. 4. Herein three kinds of N_{dose} value were the same as in Fig. 3. Compared to the results in Fig. 3(a) and Fig. 3(b), although I_{ds} values were not good enough and the variation of I_{ds} remained, the characteristics such as V_{th} uniformity improved (Fig. 4(a), (b)). Additionally, with higher N_{dose} value, further increase in I_{ds} and suppression of I_{ds} variation was confirmed (Fig. 4(c)). Moreover, an increase in μ_{FE} and decrease in R_{sh_n+} were achieved as listed below. The results showed that the film property of PAS-SiN should be chosen adequately.



	(a)	(b)	(c)
μ_{FE} [cm²/Vs]	2.0	1.2	11.2
V_{th} [V]	1.9	2.5	4.0
R_{sh_n+} [kΩ/sq]	3.8	4.5	1.4

Figure 4. I_{ds}–V_{gs} transfer characteristics of TGSA oxide TFTs (W/L = 3/2 μm) with different N_{dode} values of (a) low, (b) middle, and (c) high. The average values of electrical characteristics of those TFTs were listed below. PAS-SiN was deposited under high-hydrogen-content condition.

Based on these results, the following phenomenon possibly occurs in ion-implanted n^+ oxide regions. In the previous paper, low resistance of the oxide film seems to be caused by the presence of a large amount of hydrogen trapped in oxygen vacancies (VoH) [7]. The ion-implanted oxide layer (and the GI layer, too) was probably damaged. As a result, it was inferred that some oxygen vacancies (Vo) could be generated in the n^+ oxide regions. Therefore, the incorporation of hydrogen in such Vo results in the formation of VoH, and consequently R_{sh_n+} becomes low.

Furthermore, from the viewpoint of control of the intrinsic channel region in the TGSA oxide TFT, the effectivity of the high dose in S/D regions is described. Figure 5 shows I_{ds}-V_{gs} transfer characteristics of the TGSA oxide TFT with shorter L (1.75 μm). These TFTs were fabricated by using two different N_{dose} values, which were the same as in Fig. 4(b) and 4(c), respectively. The deposited PAS-SiN film with high hydrogen content was also the same as in Fig. 4. When the N_{dose} had the middle value, the conductive characteristic was observed (Fig. 5(a)). Besides, in the case of high N_{dose} value, a significant shift of the characteristic in the negative V_{gs} direction was not exhibited (Fig. 5(b)). According to the previous report, it was suggested that the effective channel length, which was calculated by the transmission line method, should be reduced by hydrogen diffusion from surrounding layers [8]. In the ion-implanted S/D regions, such hydrogen seems to be trapped in Vo. Therefore, hydrogen diffusion into the intrinsic channel region could be suppressed. Consequently, the V_{th} shift in the negative direction was assumed to be suppressed by the high dose of I/I.

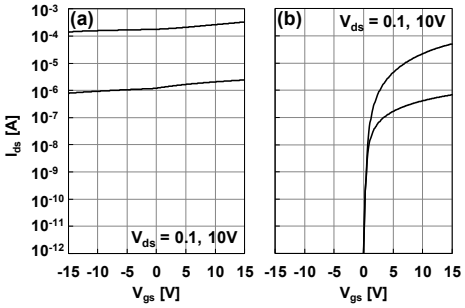


Figure 5. I_{ds}–V_{gs} transfer characteristics of TGSA oxide TFTs (W/L = 3/1.75 μm) with different N_{dode} values of (a) middle, and (b) high. PAS-SiN was deposited under high-hydrogen-content condition.

Finally, to understand the feasibility of the TGSA oxide TFTs developed in this study, the V_{th} of the optimized TFTs was investigated as a function of measured L, as shown in Fig. 6. While V_{th} barely changed at L >1.5 μm, it decreased markedly in the case of L <1.5 μm. This result indicates that L = 2.0 μm is sufficient length for obtaining good TFT characteristics, considering the fluctuation in L. This can likely be attributed to the fact that the S/D regions were determined by self-aligned I/I through GI with a gate metal mask.

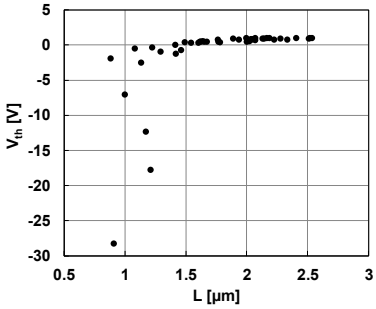
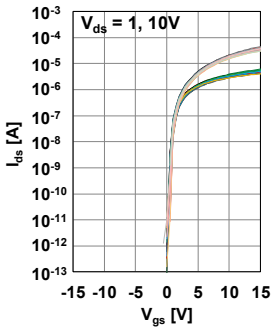


Figure 6. V_{th} of TGSA oxide TFTs as a function of measured L.

In fact, to adopt the advanced LTPS TFT technology for high-end LCDs, the electrical characteristics of oxide TFTs were further adjusted under additional considerations, compared to those listed in Fig. 4(c). Consequently, appropriate characteristics were successfully achieved for the practical operation of each pixel, as shown in Fig. 7 [6].



μ_{FE} [cm²/Vs]	9.5
V_{th} [V]	0.44
σV_{th} [V]	0.26

Figure 7. I_{ds}–V_{gs} transfer characteristics of optimized TGSA oxide TFTs with W/L = 3/2 μm

3.3 Reliability of optimized TGSA oxide TFT

As mentioned earlier, the reduction of the V_{th} shift under NBTIS condition is important for oxide TFTs because the negative duty ratio is considerably higher than the positive one in LCDs. Thus, the I_{ds}-V_{gs} transfer characteristics of the fabricated TGSA oxide TFT before and after NBTIS were investigated, as shown in Fig. 8. To realize highly reliable LCDs, the deposition conditions of GI were optimized although both N_{dose} value and PAS-SiN film property was the same as those in Fig. 4(c). During NBTIS, the gate voltage of −13.3 V, which was

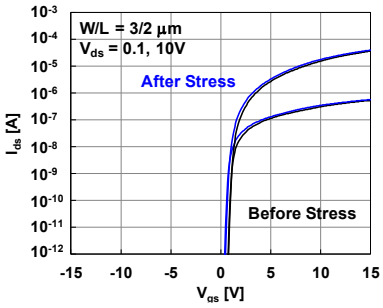


Figure 8. I_{ds}–V_{gs} transfer characteristics of TGSA oxide TFTs under optimized CVD conditions of the GI before and after NBTIS. Stress conditions were Temp. = 60 °C, V_{gs} = −13.3 V, V_d = V_s = GND, and stress time = 3600 s under 8000 cd/m^2 (with illumination from the bottom of the TFT).

determined by the voltage of LCD operation, was applied at 60 °C for 3600 s. Backlight illumination of 8000 cd/m^2 was irradiated from the bottom of the TFT. Despite applying stress for 3600 s, a large V_{th} shift toward the negative gate voltage direction was not exhibited, and the V_{th} shift had a considerably small value of −0.28 V. The previous paper reported that the defect states in the oxide and SiO_2 film seem to affect the NBTIS degradation of oxide TFTs [10]. This improvement in the V_{th} shift was probably due to the reduction of plasma damage to the oxide layer during GI deposition.

4 CONCLUSIONS

Advanced LTPS TFT technology with a TGSA oxide TFT was developed on the Generation 6 mother glass substrate. The S/D regions of the oxide TFTs were fabricated by using I/I. The characteristics of the LTPS TFTs were appropriate for peripheral circuit operation. Furthermore, by adopting adequate processing conditions, the oxide TFTs with short L enabled the required performance for pixel TFTs in LCDs. The optimized oxide TFT exhibited good reliability under NBTIS. These results indicate that the advanced LTPS TFT technology has promising prospects as the backplane for high-end LCDs.

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