Fabrication of Top-Gate Self-Aligned Amorphous InGaSnO TFTs with High Mobility

Nian Liu[2] , Huafei Xie[1]*, Xueru Mei[2], Macai Lu[2], Lei Wen[2], Shujhih Chen[2], Shengdong Zhang[1], Chiayu Lee[2], Xin Zhang[2]

[1]School of Electronic and Computer Engineering, Peking University, Shenzhen, China 518055
[2]Shenzhen China Star Optoelectronics Semiconductor Display Technology Co., Ltd, Shenzhen, China 518132

Key words:Indium Gallium Tin Oxide (IGTO), High Mobility, Deposition Condition, top-gate(TG) self-aligned(SA)

Abstract

The effect of deposition condition of dielectric layer on top-gate self-aligned amorphous InGaSnO TFT have been discussed, higher N_2O/SiH_4 gas ratio and medium power are better. The resulting a-IGTO TFT at Gen.4.5 glass exhibited good uniformity and high mobility of 28.57cm^2/Vs, sweep swing of 0.27 V/decade, threshold voltage of 0.53V.

1 Introduction

Amorphous InGaZnO have been widely used in flexible、transparent and OLED display for high mobility （~10 cm^2/Vs）、high transmittance（>90%） and good machine behavior. Comparing to organic LEDs (OLEDs) or liquid crystal displays (LCDs), which are conventionally used as light sources for displays, inorganic LEDs have many advantages such as low power consumption, high brightness, short response time, and long lifetime [1]. To achieve higher brightness and narrow bezel , it's necessary to study high mobility TFT for micro LED display. In this work, we successfully demonstrate a-IGTO TG-SA TFT at Gen. 4.5 glass with a high mobility of 28.57cm^2/Vs.

2 Experiment

The structure and SEM image of top-gate self-aligned a-IGTO TFTs is showed in **Fig. 1**. They were fabricated on Gen 4.5 glass. Firstly, a light-shielding metal (LS) was deposited and patterned on substrate. Secondly, a SiOx buffer layer was deposited by plasma enhanced chemical vapor deposition (PECVD). Then after anneal at 320℃ for 1hour 30nm a-IGTO with high content of In was deposited by DC sputtering, and defined through photolithography and wet etching after annealed. SiOx layer was deposited by PECVD as the gate insulator (GI) . Mo/Al/Mo metal layers were deposited using DC sputtering as the gate layer. Gate and GI layer were continuously patterned to form top-gate self-aligned structure. Plasma treatment was applied for creating n+ IGTO S/D ohmic contact. After inter-layer dielectrics deposition (ILD), Mo/Al/Mo metal layers were deposited and patterned as the source (S) and drain (D). Devices fabrication were finished by passivation (PV) layer deposition. Keithley 4200-SCS semiconductor parameter analyzer was used to measure device electrical properties in the dark.

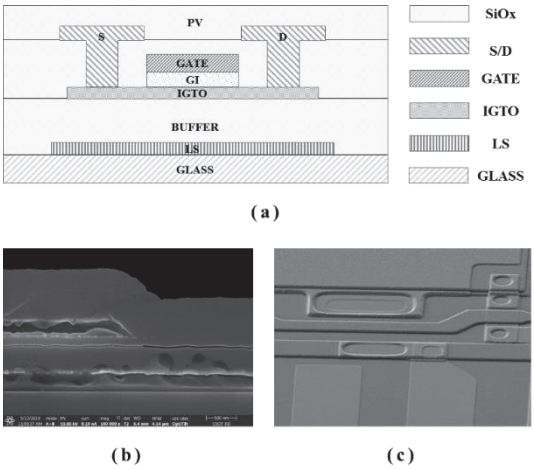

Fig. 1 The structure(a) , cross section(b) and top-view(c) of TG-SA IGTO TFT

3 Results and discussion

Previous work showed SiOx (Buffer, GI and ILD) deposition condition is very important for TG-SA a-IGZO TFT, excessive O (O_{ex}) or hydrogen in SiOx can diffuse after thermal annealing, and O_{ex} and hydrogen content in active layer and the interface of active-GI greatly influence the characteristic of TFT[2~4]. To optimize the characteristic of TFTs we designed different Buffer, GI and ILD deposition conditions and measured Id-Vg at different sites of Gen.4.5 glass.

3.1 Buffer deposition condition

As **Table 1** ,sample A/B/C were fabricated with the same condition of IGTO and ILD, but with different buffer and ILD gas flow ratio. **Fig. 2** is the IdVg curve, it showed sample B and sample C which fabricated with relatively lower N_2O:SiH_4 ratio GI layer were short, the shortage may attribute to hydrogen diffused in SiOx deposition

process and anneal process. That means TG-SA a-IGTO TFTs are more sensitive to GI condition than buffer. IGTO TFTs are also sensitive to the hydrogen content, hydrogen in active layer brings a large number of free electronics and leads to shortage of device[5,6] , just like IGZO. Buffer of lower N_2O:SiH_4 ratio contain higher hydrogen content in SiOx, but after 1hour high temperature (320℃) anneal process in clean and dry air atmosphere, hydrogen diffused to surface and escape from buffer. Thus deposition condition of buffer have not significant influence on device properties comparing to GI. High N_2O:SiH_4 ratio GI deposition is necessary for prevent shortages.

Table 1 Buffer deposition condition of sample A/B/C

Sample	A	B	C
Buffer	Low N_2O:SiH_4 ratio	Medium N_2O:SiH_4 ratio	High N_2O:SiH_4 ratio
IGTO	High O_2/(O_2+Ar) ratio		
GI	High N_2O:SiH_4 ratio	Medium N_2O:SiH_4 ratio	Low N_2O:SiH_4 ratio
	Medium Deposit Power		
ILD	High N_2O:SiH_4 ratio		

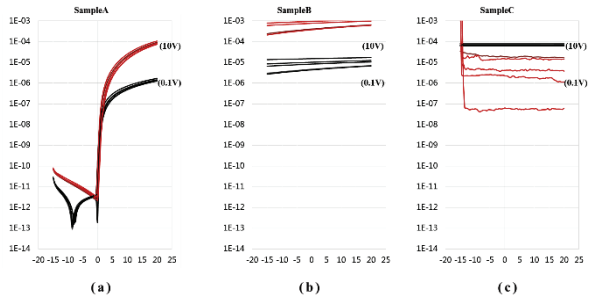

Fig. 2 The Id-Vg curve with (a)Buffer low N_2O/SiH_4 ratio and GI high N_2O/SiH_4 ratio .(b) Buffer medium N_2O/SiH_4 ratio and GI medium N_2O/SiH_4 ratio . (c) Buffer high N_2O/SiH_4 ratio and GI low N_2O/SiH_4 ratio .

3.2 GI deposition condition

Secondly, we designed an experiment to search how GI deposition power influence on TG-SA TFTs. As **Table 2** ,sample D/E/F were fabricated with low/medium/high GI deposition power respectively. **Fig.3** is the IdVg transfer curve of three samples, sample D with low deposition power has a short, and sample E shows better uniformity than sample F. Film formation rate is faster at lower deposition power , and it results in more hydrogen residual in SiOx, that leads to shortage as sample D. Besides, higher power enhanced energy of plasma, more weak bond, like Si-H, was impacted by plasma, so higher power can get more compact SiOx (as **Fig.4**). So higher power GI (Sample E) shows good properties of no shortages and lower SS comparing to low power GI (Sample D). But excessive deposition power (Sample F) would cause nonuniformity thin film characteristic, and excess oxygen reduced mobility and increased defect at the interface of active-GI which raised SS.

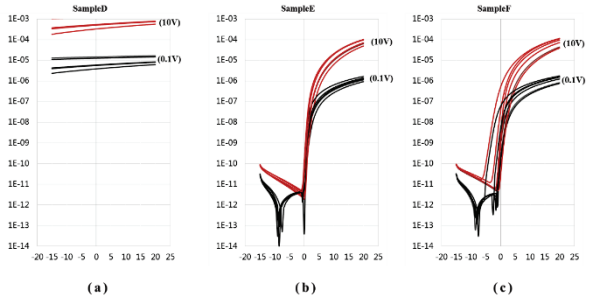

Fig. 3 The Id-Vg curve with(a)GI low power.(b) GI medium power. (c) GI high power.

Table 2 GI deposition condition of sample D/E/F

Sample	D	E	F
Buffer	Low N_2O:SiH_4 ratio		
IGTO	High O_2/(O_2+Ar) ratio		
GI	Medium N_2O:SiH_4 ratio		
	Low Deposition Power	Medium Deposition Power	High Deposition Power
ILD	High N_2O:SiH_4 ratio		

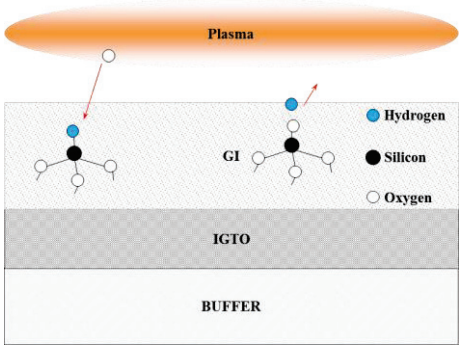

Fig. 4 The diagrammatic sketch of weak bond broken in SiOx:H during deposition

3.3 ILD deposition condition

ILD layer directly contacts with the conductive IGTO, the influence of ILD was also searched, as **Table 3** ,sample E/G were fabricated with high and low ILD deposition gas flow respectively. **Fig. 5** shows low ratio of N2O:SiH4 (Sample G) TFTs were entire shorted at different sites, while high N2O:SiH4 ratio (Sample G) TFTs got good performance. Reduced hydrogen in ILD via increased N2O:SiH4 ratio during deposition can decrease diffusion of hydrogen into IGTO and prevent shortages of TFTs.

Table 3 ILD deposition condition of sample E/G

Sample	E	G
Buffer	Low N_2O:SiH_4 ratio	
IGTO	High O_2/(O_2+Ar) ratio	
GI	Medium N_2O:SiH_4 ratio	
	Medium Deposit Power	
ILD	High N_2O:SiH_4 ratio	Low N_2O:SiH_4 ratio

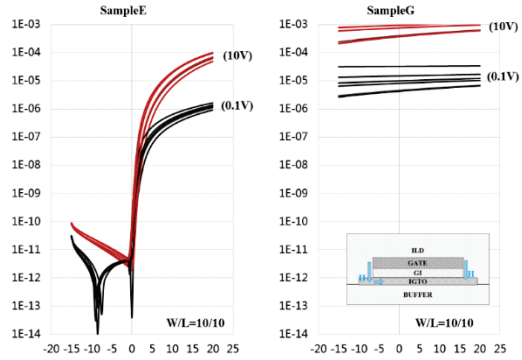

Fig. 5 The Id-Vg curve with (a)ILD high N_2O/SiH_4 ratio .(b) ILD low N_2O/SiH_4 ratio.

3.4 Result

Finally, we demonstrate a-IGTO TG-SA TFTs with a high mobility of 28.57 cm^2/Vs, sweep swing of 0.27 V/decade, threshold voltage (V_{th}) of 0.53V ,and good uniformity at Gen. 4.5 glass (as **Table 4** ,sample A) . The bias stress stabilities of sample A were also measured at +30V 60℃ for 2000s (PBTS),and -30V 60℃ at 4500nits white light for 2000s (NBTIS), the Vth shift of PBTS was 3.17V and NBTIS was -4.95V. the high mobility a-IGTO TFTs showed good uniformity and comparative performance of bias stress stability to a-IGZO(as **Fig.6**).

4 Conclusion

We successfully demonstrate TG-SA TFT with high mobility and good uniformity at Gen.4.5, and discuss effect of process condition of dielectric layer . TG-SA a-IGTO TFTs are sensitive to Buffer, GI and ILD deposition conditions, and higher N_2O:SiH_4 ratio and medium deposition power are better for TFT characteristic.

Table 4 Electrical parameters of sample A, B, C, D, E, F and G

Sample	A	B	C	D	E	F	G
Mobility (cm^2/Vs)	28.57	/	/	/	29.19	26.21	/
SS (V/decade)	0.27	/	/	/	0.39	0.50	/
Vth (V)	0.53	/	/	/	0.74	-0.65	/
ΔV_{th} (V)	0.88	/	/	/	1.26	5.00	/

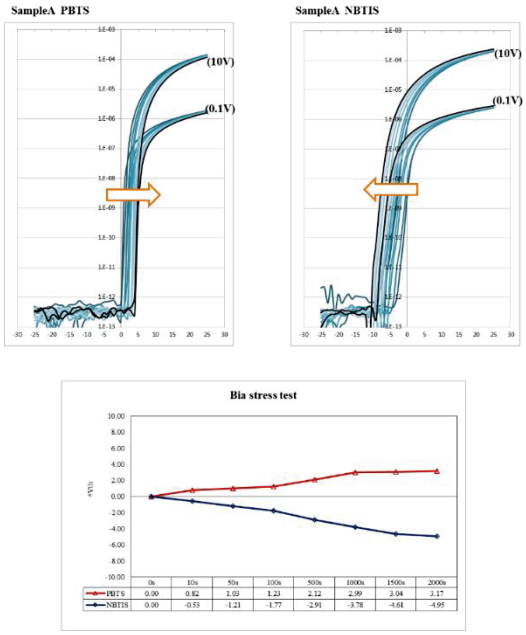

Fig. 6 The positive and negative bias stress test of sample A

Acknowledgment

*These authors contributed equally to this work

References

[1] Bonar, James Ronald, et al. "High-brightness low-power consumption microLED arrays." Proceedings of SPIE (2016).

[2] J. M. Lee, I. T. Cho, J. H. Lee, W. S. Cheong, C. S. Hwang, and H. I. Kwon, “Comparative study of electrical instabilities in top-gate InGaZnO thin film transistors with Al2O3 and Al2O3/SiNx gate dielectrics” Appl. Phys. Lett. 94, 222112 (2009).

[3] Li H, Guo Y, Robertson J, et al. Hydrogen and the Light-Induced Bias Instability Mechanism in Amorphous Oxide Semiconductors[J]. Scientific Reports, 2017, 7(1).

[4] Nomura, Kenji, Toshio Kamiya, and Hideo Hosono. "Effects of Diffusion of Hydrogen and Oxygen on Electrical Properties of Amorphous Oxide Semiconductor, In-Ga-Zn-O." ECS Journal of Solid State Science and Technology 2.1 (2013).

[5] Mitsuru Nakata, Mototaka Ochi, et al.” Fabrication of a Short - Channel Oxide TFT Utilizing the Resistance Reduction Phenomenon in In-Ga-Sn-O. ” SID 2017 DIGEST • 1227(2017)

[6] Nomura, Kenji, Toshio Kamiya, and Hideo Hosono. "Effects of Diffusion of Hydrogen and Oxygen on Electrical Properties of Amorphous Oxide Semiconductor, In-Ga-Zn-O." ECS Journal of Solid State Science and Technology 2.1 (2013)