New 3.5T2C Pixel Circuit with Symmetrical Structure for 3D AMOLED Displays

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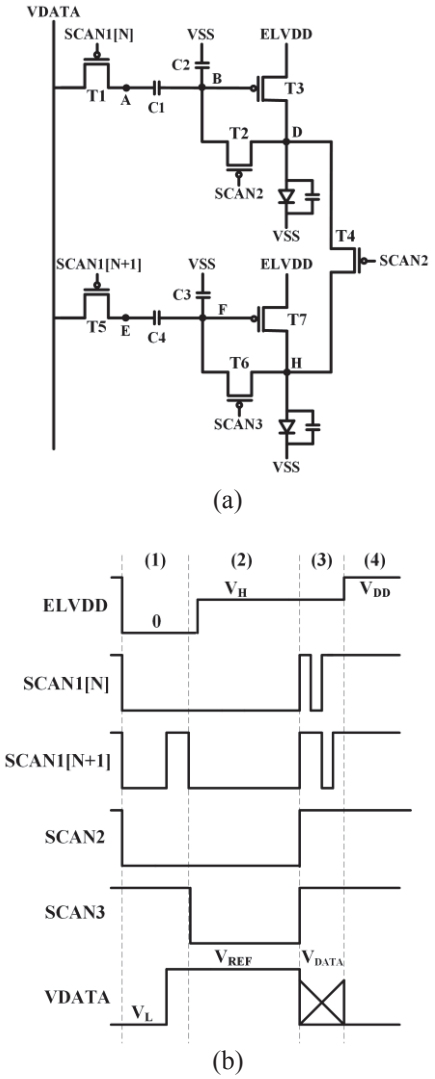
ABSTRACT

This paper proposes the 3.5T2C pixel circuit compensating for threshold voltage (V_{TH}) variation of LTPS-TFTs and preventing image flicker. Simulation results show that the relative current error rates under V_{TH} variations are all below 4.37 %. Furthermore, OLEDs are turned off during the programming period, thereby achieving flicker-free images.

1 INTRODUCTION

Three-Dimensional (3D) AMOLED display is a practical way to present 3D images to human eyes because of the fast response time of OLEDs [1], [2]. Among several types of 3D AMOLED displays, VR head-mounted displays are the current trend of the display industry nowadays. Low temperature poly-silicon thin-film transistors (LTPS-TFTs) are usually used in pixel circuits of high-resolution and small / medium-size 3D AMOLED displays because of their high mobility [3], [4]. Nevertheless, their unavoidable threshold voltage (V_{TH}) variation of LTPS-TFTs leads to OLED currents fluctuation between pixels, decreasing the uniformity of images [5]. To ameliorate the image quality, Chang *et al.* proposed a pixel circuit for 3D AMOLED display [6]. This paper utilizes diode-connected structure and simultaneous emission (SE) driving method to successfully compensate for V_{TH} variation of LTPS-TFTs and produce uniform 3D images. However, the structure of this pixel circuit is complicated, consisting of five TFTs, two capacitors and four control signal lines, resulting in larger layout area. In the compensation period of this pixel circuit's operation, a large compensation current flowing through OLED leads to flicker phenomenon, reducing the contrast ratio and increasing additional power consumption of displays. Therefore, the issues of this pixel circuit mentioned above increase the difficulty of realizing high-resolution and small / medium-size 3D AMOLED displays such as VR head-mounted displays.

To meet the major requirements of realizing VR head-mounted display, namely V_{TH} compensation of LTPS-TFTs, small layout area of pixel circuit and prevention of flicker phenomenon, this work proposes a new pixel circuit with a simple structure combining two pixels of adjacent rows into one circuit for simplifying the circuit structure to 3.5-TFTs, two capacitors and two control signal lines per pixel. Furthermore, the proposed work adopts SE driving method for producing 3D images, and effectively compensates for V_{TH} variation of LTPS-TFTs through utilizing capacitive coupling effect, charge sharing effect and symmetrical diode-connected structure. This work also turns off the OLEDs during the programming period, thereby preventing the flicker



Figs. 1 Proposed AMOLED pixel circuit. (a) Schematic. (b) Timing diagram.

phenomenon. Simulation results indicate that the relative OLED emission current error rates over entire data range (4.4 V ~ 5.2 V) are less than 4.37 % as the V_{TH} of LTPS-TFTs varies ±0.5 V.

2 CIRCUIT SCHEMATIC AND OPERATION

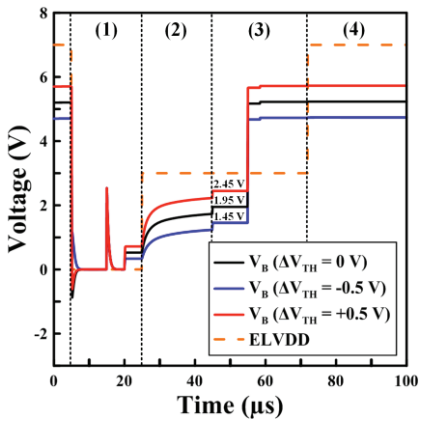
Figs. 1 (a) and (b) plot the schematic and timing diagram of proposed circuit comprising two driving TFT (T3 and T7) for driving OLED, five switching TFTs (T1, T2, T4, T5, and T6), four capacitors (C1, C2, C3 and C4) for storing data voltages, and three control signals (SCAN1[N], SCAN1[N+1], SCAN2 and SCAN3), which shared by two pixels. SCAN1[N] and SCAN1[N+1] are used to control T1 and T5 for resetting the voltage of node A and E and applying the data voltage (V_{DATA_N} / V_{DATA_N+1}) to them, respectively. SCAN2 and SCAN3 are used to control T2, T4 and T6 for resetting the voltage nodes and compensating for the V_{TH} variation of driving TFTs. The layout area of each pixel is 3.5-TFTs, two capacitors and two control signal lines. The operation of proposed pixel circuit is separated into four periods, namely reset period, compensation period, data input period and emission period, which are described as follows.

(1) Reset period: In this period, SCAN1[N] is low to turn on T1 for resetting the voltage of node A to V_L through VDATA. SCAN2 is low to turn on T2 and T4 for resetting the voltages of node B, D and H. SCAN3 is high to turn off T6 for separating node F, namely the gate of T7, from other nodes. Data voltage (VDATA) is adjusted to a lower voltage -6 V to dramatically pull down the voltage of node E and node F through capacitive coupling effect, changing T7 from a driving TFT to a switching TFT because it is operating at triode region. Node B, D and H are discharged to near 0 V through T7 for resetting the voltages of them. The voltage of OLED is less than V_{OLED_0} to turn off OLED for preventing flicker phenomenon. In this period, all pixels of the display are reset at the same time because of adopting SE driving scheme.

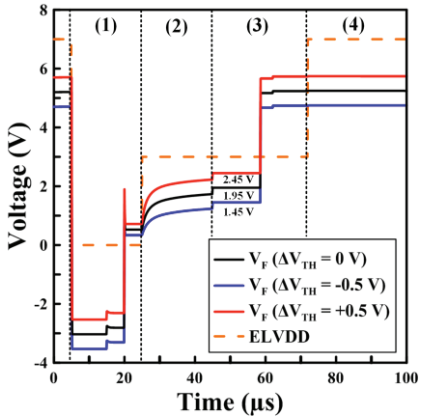
$$Frame[M-1]:$$
$$ELVDD = V_{DD},\ V_{F\_Emission} = V_X$$
$$Frame[M]:$$
$$ELVDD = 0\,V,$$
$$V_{F\_Reset} = V_X + \frac{C4}{C3+C4}(V_L - V_{DATA[M-1]})$$

where $V_{F\_Emission}$ is the voltage of node F in emission period of the [M-1]th frame, V_X is a unfixed voltage containing various data voltages, V_{F_Reset} is the voltage of node F in reset period of the [M]th frame, and $V_{DATA[M-1]}$ is the data voltage in data input period of the [M-1]th frame.

Then, T5 is turned off by SCAN1[N+1] and V_{DATA} turns to V_{REF}. The voltage of C1 charges to V_{REF} – 0 V in the end of the reset period.



(a)



(b)

Figs. 2 Transient waveforms of (a) node B (b) node F of proposed pixel circuit as V_{TH} varies ±0.5 V

(2) Compensation period: At the beginning of this period, SCAN1[N+1] goes low to turn on T5, and voltage of node E is reset to V_{REF} through VDATA.SCAN3 goes low to turn on T6 for making the initial voltage of V_{TH} compensation identical in both pixels. Then ELVDD is adjusted to a high voltage V_H, T3 and T7 operate at saturation region because of diode-connected structure. Voltages of nodes B and F are charged to V_H - $|V_{TH}|$ until T3 and T7 turn off, where $|V_{TH}|$ is assumed to be equal to the threshold voltage of T3 and T7. This assumption, the electrical characteristics of TFTs between adjacent pixels are regarded as nearly identical, is usually employed in previous proposed AMOLED pixel circuits [8], [9]. Both pixels are connected by T4, making the terminal voltages of nodes B and F are same. Moreover, the voltage of OLED remains lower than V_{OLED_0} to block the compensation current from flowing through OLED during this period. The compensation period is concurrently executed by all pixel circuits.

(3) Data Input period: During this period, data voltages are written in the pixels progressively row by row. After finishing V_{TH} compensation, SCAN2 and SCAN3 are high to turn off T2, T4 and T6 of all pixel

circuits. SCAN1[N] goes low to turn on T1 for applying data voltage to node A. The voltage of node B, namely the gate voltage of T3, is changed to V_H - $|V_{TH}|$ + (V_{DATA_N} - V_{REF})*(C1/C1+C2) because of capacitive coupling of C1 and C2, where V_{DATA_N} is the data voltage of the upper pixel, and the one of lower pixel is represented as V_{DATA_N+1}. The lower pixel's circuit operation in data input period is same as upper one.

(4) Emission period: After writing data in each pixel, whole panel executes the emission period simultaneously. All SCANs are high to turn off all TFTs. ELVDD turns to VDD to make sure T3 and T7 operate in saturation region, providing stable emission currents to light up OLEDs. The OLED emission currents of two pixels are calculated as

$$\begin{aligned} I_{OLED} &= \frac{1}{2}\mu C_{OX}\left(\frac{W}{L}\right)(V_{SG}-|V_{TH}|)^2 \\ &= \frac{1}{2}\mu C_{OX}\left(\frac{W}{L}\right)[V_{DD}-V_H+|V_{TH}| \\ &\quad -(V_{DATA\_N}-V_{REF})*\frac{C1}{C1+C2}-|V_{TH}|]^2 \\ &= \frac{1}{2}\mu C_{OX}\left(\frac{W}{L}\right)(V_{DD}-V_H \\ &\quad -(V_{DATA\_N}-V_{REF})*\frac{C1}{C1+C2})^2 \quad (1) \end{aligned}$$

where μ, C_{OX} and (W/L) are mobility of T3 and T7, the gate capacitance per unit area and the channel-width-to-channel-length ratio, respectively. Since V_{TH} is removed in Eq. (1), the emission currents of OLED are independent of V_{TH} variation of driving TFTs. Consequently, this pixel circuit can provide stable emission currents for achieving uniform 3D images.

TABLE 1
PARAMETERS OF PROPOSED AMOLED PIXEL CIRCUIT

Parameter	Value	Parameter	Value
ELVDD(V)	7/ 3/ 0	$(W/L)_{T3,\ T7}$ (μm/μm)	3 / 22
ELVSS (V)	-1	$(W/L)_{T1,T2,T4,T5,T6}$(μm/μm)	3 / 3
V_{DATA} (V)	4.4~5.2	$(W/L)_{TOLED}$(μm/μm)	5 / 18
V_{REF} (V)	0	C1, C4 / C2, C3 (pF)	0.3 / 0.1
V_L (V)	-6	V_{OLED_0} (V)	4
SCAN (V)	-10 /10	C_{OLED} (pF)	0.12
ΔV_{TH} (V)	±0.5		

3 RESULTS AND DISCUSSION

To verify the performance and functionality of proposed pixel circuit, simulations are conducted by HSPICE for the full high-definition displays (1920 × 1080). The frame-rate of the display is increased from 60 Hz to 240 Hz because of achieving temporal division method. The compensation period is set for 20 μs, and one data voltage writing time is 3.5 μs. The simulation parameters of power supply, ground, signal lines and devices are listed in Table 1, where ΔV_{TH} is the degree of LTPS-TFTs' V_{TH} variation, V_{OLED_0} is the threshold voltage of OLED and SCAN is the high / low voltage level of control signals. OLEDs are simulated by a diode-connected TFT (T_{OLED}) and a parallel capacitor (C_{OLED}) [7]. The simulation results are depicted and explained as follow. Figs. 2 (a) and (b) plot the transient waveform of the voltage of node B (V_B) and node F (V_F), namely the gate of upper and lower pixel. In both figures, the V_{TH} varies ±0.5 V that is effectively detected after executing the compensation period, confirming the compensation capability of proposed pixel. Shown in Fig. 3, V_B and V_F are merged into same values, 0.52 V to 1.95 V, after the reset period until they are wrote in different data voltages. To investigate the proposed circuit's functionality of preventing flicker phenomenon, Fig. 4 plots the transient waveforms of current flowing through OLED (I_{OLED}) and anode voltage of OLED (V_D) as V_{TH} varies ±0.5 V, where I_{OLED} is for high grey level images. The highest potential difference between the V_D and VSS is 3.47 V, which is less than V_{OLED_0} (4 V), thereby turning off OLED during the programming period. Hence, there is not any large and lasting current flowing through OLED until the emission period, achieving a totally black frame in the programming period without flicker phenomenon. Fig.5(a) depicts the curves of OLED emission currents under the conditions that ΔV_{TH} is 0, +0.5 V and -0.5 V, which are nearly overlapped over entire data range. To further analyze the accuracy of OLED emission currents with V_{TH} variation, the relative error rates are graphed in Fig.5(b). These error rates are

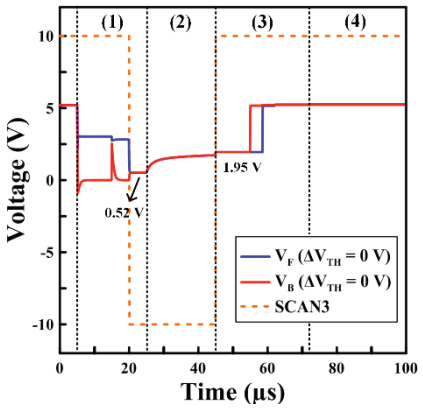


Fig. 3 Transient waveforms of charge sharing effect between voltages of nodes B and F

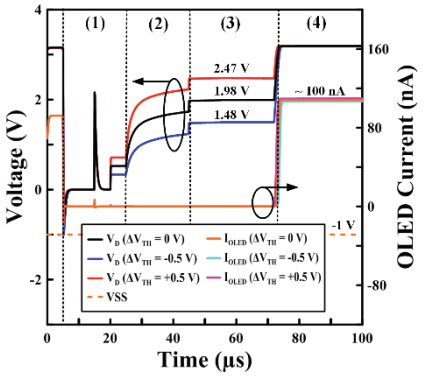
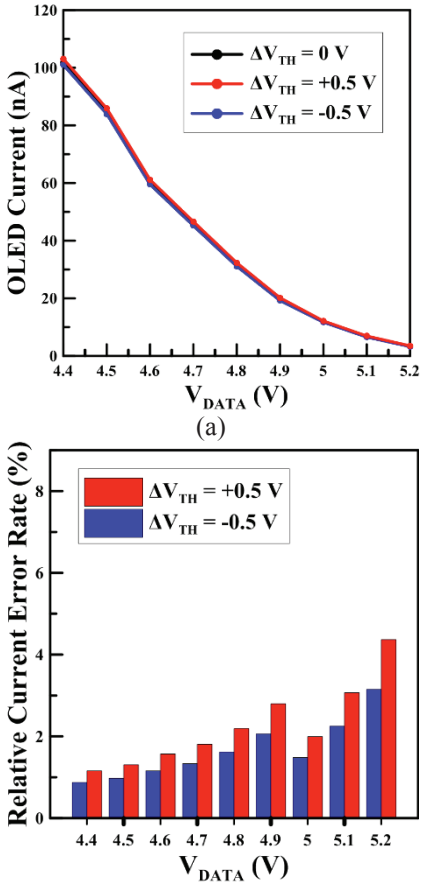


Fig. 4 Transient waveforms of current flowing through OLED and node D as V_{TH} varies ±0.5 V for high grey level images

all under 4.37 % at various data voltages. The simulation results demonstrate that the methods of proposed pixel circuit successfully compensate for the V_{TH} variation of LTPS-TFTs. Hence, the proposed pixel is suitable for high-resolution and small / medium-size 3D AMOLED displays owing to its simple structure and functions of compensating for V_{TH} variation of LTPS-TFTs and preventing flicker phenomenon.



Figs. 5 (a) OLED currents versus data voltages and (b) relative current error rates as V_{TH} varies ±0.5 V

4 CONCLUSION

Considering the application of small / medium-size high-resolution 3D AMOLED displays, this work combines two pixels of adjacent rows into one circuit for simplifying the circuit structure to 3.5T2C. Simulation results demonstrate that the relative error rates of OLED emission current are all less than 4.37 % within entire data range. Furthermore, these results show that there is not any large current flowing through OLED during the programming period, thereby validating proposed circuit's V_{TH} compensation capability and function of flicker prevention.

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