# Investigation of Hump Phenomenon in a-IGZO Thin-Film Transistors under Positive Bias Stress

Xinlv Duan[1,2], Xuewen Shi[1,2], Congyan Lu[1], Yue Su[1,2], Hansai Ji[1], Qian Chen[1,2], Di Geng[1], Ling Li[1] and Ming Liu[1]

[1] Key Laboratory of Microelectronics Devices & Integrated Technology, IMECAS, Beijing, China
[2] University of Chinese Academy of Sciences, Beijing, China
Keywords: a-IGZO TFT, positive bias stress, hump phenomenon, parasitic channel

**ABSTRACT**

*The hump phenomenon in InGaZnO thin-film transistors (IGZO TFTs) under positive bias stress (PBS) has been investigated by varying channel width and extended length. The results show that the parasitic channel is located at the edge area of the active region along the spreading current direction.*

## 1 INTRODUCTION

Amorphous In-Ga-Zn-O thin-film transistors (a-IGZO TFTs) have attracted much attention because of their good characteristics such as high mobility, high uniformity and low-temperature processing [1]. However, the stability issues of a-IGZO TFTs remain an obstacle for its further commercial application [2] [3]. As a common reliability issue, the hump phenomenon caused by positive bias stress (PBS) has been widely investigated. Generally, this phenomenon is explained as the superposition of main channel current and parasitic channel current [4]. Nevertheless, the exact location of the parasitic channel has not been pointed out yet. In this paper, the hump phenomenon in a-IGZO TFTs under PBS is studied by varying the channel width (W) and the extended length ($L_E$). The results show that the parasitic channel induced by PBS is located in the edge area of the active region along the channel length direction.

## 2 EXPERIMENT AND RESULTS

### 2.1 Hump Phenomenon in devices with different channel widths

The IGZO TFT samples were fabricated by back-channel-etched (BCE) process. Fig.1 shows the transfer characteristics of the IGZO TFTs with different W and fixed channel length (L = 10 μm) after 1000-seconds PBS ($V_{GS}$ = 15 V, $V_{DS}$ = 0 V). The transfer curves in Fig.1 can be divided into two parts, the subthreshold region (-10.5 V ≤ $V_{GS}$ ≤ -1.5 V) and the above subthreshold region (-1.5 V ≤ $V_{GS}$ ≤ 15 V), the current in these two parts shows different characteristics in transistors with different channel widths. For the above subthreshold region, the maximum current increases with W increases. But for the subthreshold region, current shows W-independence.

The hump phenomenon in the subthreshold region is generally interpreted as the presence of parasitic channel current, which means that after the PBS, a parasitic channel appears in the TFT device, and therefore, in a single TFT device, there are two transistor channels, main channel and parasitic channel [4]. The superposition of the main channel current and the parasitic channel current results in the different growth trend of the current in the subthreshold region and the above subthreshold region. The main channel is considered as a transistor with relatively large threshold voltage and maximum current, which is the main part of the above subthreshold region current, while the parasitic channel is considered as a transistor whose threshold voltage and maximum current are relatively small, which is the majority source of the current in the subthreshold region. In Fig.1, the subthreshold region current does not increase with increasing W, indicating that the parasitic channel size does not change as the actual channel size increases. Therefore, the parasitic channel is probably located in a particular portion of the actual channel, rather than being distributed throughout the entire channel region.

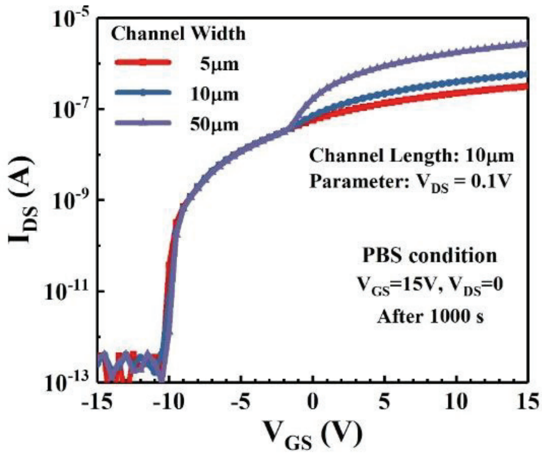


**Fig. 1 Transfer characteristics of a-IGZO TFTs with different Channel Widths after 1000s PBS**

### 2.2 Hump Phenomenon in devices with different structures

To further determine the exact location of the parasitic channel, two different structures of TFT devices were fabricated for more measurements. For device type A, as shown in Fig.2(a), the width of S/D region is larger than

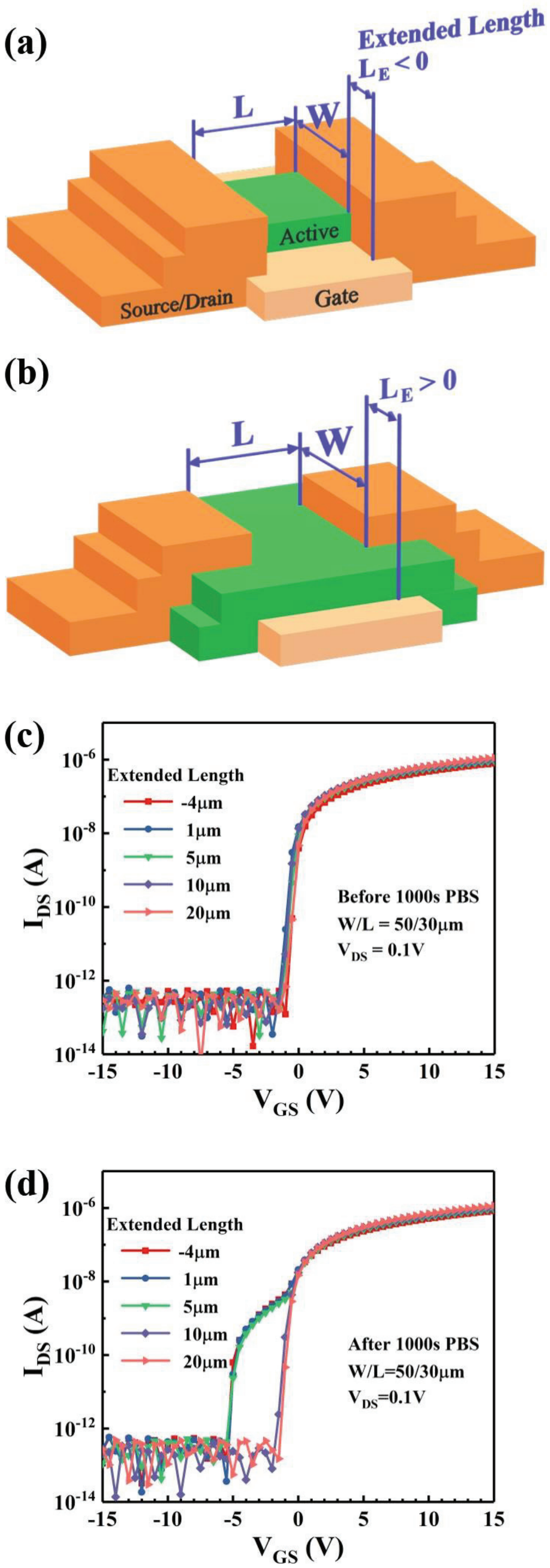


**Fig. 2 Three-dimensional structure diagram of (a) device type A and (b) device type B; Transfer characteristics of TFTs with varying $L_E$ (c) before and (d) after 1000s PBS**

the width of active region, W is defined by the width of active region. For device type B, W is defined by the width of S/D region, as shown in Fig.2(b). The length of the active area beyond the S/D area is defined as the extended-length ($L_E$). The channel size of these two types of devices is set to a fixed value (W/L = 50μm/30μm) while the actual width of the active region and the source/drain (S/D) regions is different, depending on the channel-width definition in these two types of devices. The transfer characteristics of these devices before and after 1000-seconds PBS are presented in Fig.2(c) and Fig.2(d), separately. For the devices with $L_E \geq 10$μm, there is no obvious change between the transfer curve before and after PBS, while for the devices with $L_E \leq 5$μm, obvious hump can be observed after PBS.

## 3 DISCUSSION

The measurement results as shown above can be explained by electric field coverage shown in Fig.3.

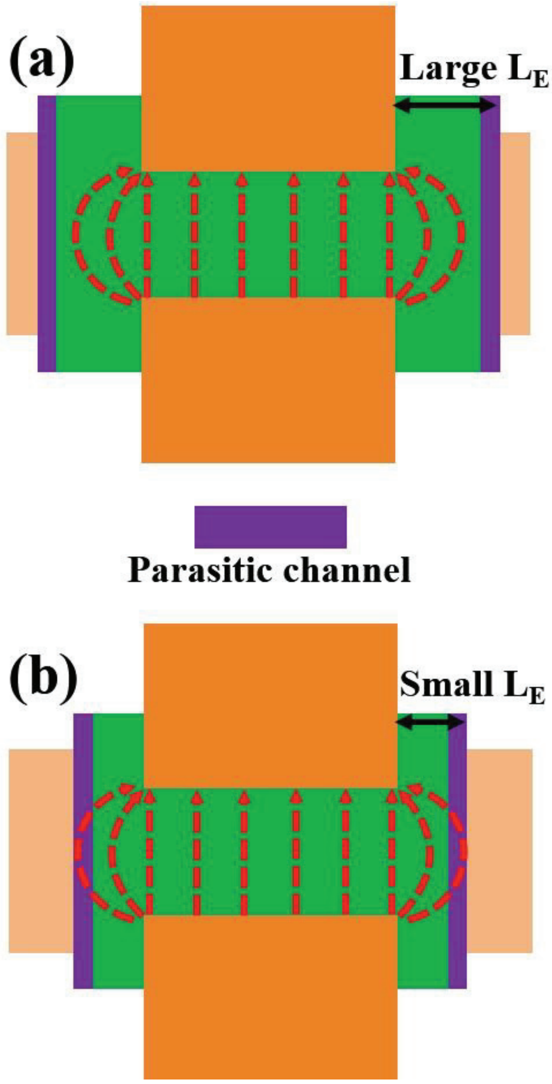


**Fig. 3 Electric field coverage in a-IGZO TFTs with (a) large $L_E$ and (b) small $L_E$**

When a voltage is applied between source and drain, the real width of the electric field applied in the active area is larger than the width of the source and drain. If the parasitic transistors are located at the edge of active layer, when $L_E$ is long enough, the extended electric field cannot reach the edge region of the active area (Fig.3(a)), but if $L_E$ is small, the extended electric field can cover the whole edge part of the active region (Fig.3(b)). Thus, under former condition, the lateral electric field cannot drive electrons in parasitic transistors flowing between source and drain electrodes; while in later one, electrons at edge of active layer could be easily affected by lateral electric field and hump phenomenon appears.

## 4 CONCLUSIONS

Generally, the hump phenomenon induced by PBS is explained as the superposition of main channel current and parasitic channel current [4]. Nevertheless, the exact location of the parasitic channel has not been pointed out yet. In this paper, the exact location of the parasitic channel was located for the first time by varying the channel width and the extended length. The results imply that parasitic edge transistors induced current is responsible for the hump phenomenon of the transfer characteristic. According to our conclusion, the hump effect can be suppressed by enlarge the width of the active layer, which will improve the stability of the device. This improvement will promote the application of a-IGZO TFT in high reliability circuits.

## REFERENCES

[1] K. Nomura, H. Ohta, A. Takagi, T. Kamiya, M. Hirano, and H. Hosono, "Room-temperature fabrication of transparent flexible thin-film transistors using amorphous oxide semiconductors", Nature, vol. 432, pp. 488-492, Nov. 2004

[2] M. D. H. Chowdhury, P. Migliorato, and J. Jang, "Light induced instabilities in amorphous indium–gallium–zinc–oxide thin-film transistors," Appl. Phys. Lett., 97.17 (2010): 173506.

[3] A. Suresh and J. Muth, "Bias stress stability of indium gallium zinc oxide channel based transparent thin film transistors," Appl. Phys. Lett., 92.3 (2008): 033502.

[4] M. Mativenga, M. Seok, and J. Jang. "Gate bias-stress induced hump-effect in transfer characteristics of amorphous-indium-gallium-zinc-oxide thin-film transistors with various channel widths." Appl. Phys. Lett. 99.12 (2011): 122107.