Effect of Ambient Atmosphere on Abnormal Degradation Behavior in Metal-Oxide Thin-Film Transistor under Positive Gate-Bias and Temperature Stress

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ABSTRACT

Positive gate-bias and temperature stress were performed on the respective metal-oxide thin-film transistors as fabricated and stored in air ambiance for three months. An abnormal negative shift of the transfer characteristics was observed, and a channel width-dependence of device degradation occurred after long-term storing.

1 INTRODUCTION

Large-area and high-resolution active-matrix displays (AMDs) require the thin-film transistors (TFTs) with high mobility, low leakage current and high uniformity as their pixel driving devices. Beyond Si-based semiconductors, metal-oxide (MO) such as zinc oxide and its variant indium-gallium-zinc oxide (IGZO), profited from their superiorities [1], have emerged as the most promising channel materials for TFTs being applied in flat-panel displays nowadays [2]. However, MO TFTs are still faced with reliability issues [3], especially when under negative-bias and illumination stress (NBIS) [4] and positive gate-bias and temperature stress (PBTS) [5]. The fragile and crummy device performance after these stresses hinders the technology ready for wider industrial adaptation.

Revealed by the dependence of the shift (ΔV_{on}) of turn-on voltage (V_{on}) and the subthreshold-swing change (ΔSS) on the stress duration, a PBTS-induced positive ΔV_{on} without any ΔSS in transfer characteristics are mostly reported and attributed to the trapping of electrons at the channel/gate insulator interface [6]. However, an abnormal negative [7-10] or bidirectional shift [11] with a ΔSS of transfer curves have also been observed. The behavior of a negative ΔV_{on} is usually attributed to the effect of stress-created donor-liked defects or trapping of positive charges. But due to the existence of massive electrons in the channel under PBTS, the second hypothesis is not feasible for this situation. For the mechanism of defects creation, the study normally concentrates on fresh devices but sheds little light on the rich implications from “old” devices.

In this work, metal-oxide TFTs with thermally-induced source/drain (S/D) regions were fabricated to investigate the TFT reliabilities against positive gate-bias and temperature stress. Benefited from the oxidized high-quality silicon-oxide serving as the gate insulator and etch-stop interface layer, PBTS-induced negative ΔV_{on} was observed in the stress-time-evolution of transfer characteristics. It shows that a severer degradation and a channel-width dependence occurred for devices after storing in ambient. Hydrogen-related defects such as hydroxyl groups (OH^-) are assumed to be the role. It’s the first time that the effect of ambient atmosphere for such long-term was researched and the correlated activation energy was extracted.

2 EXPERIMENT

The fabrication of a TFT started with the sputter-deposition and patterning of ~80 nm molybdenum (Mo) as the bottom gate on an oxidized silicon wafer. A gate insulator (GI) stack consisting of 50 nm silicon nitride topped with 75 nm silicon oxide (SiO_x) was deposited in a plasma-enhanced chemical vapor deposition reactor (PECVD). Silane, hydrogen, and nitrous oxide were employed as the reaction source for SiO_x. The SiO_x deposition frequency, power, and pressure are 13.56 MHz, 60 W, and 90 mtorr respectively. Then oxidizing annealing at 400 °C in pure oxygen (O_2) for 2 hours was adopted for dehydrogenation and oxide solidification, thus improving the interface quality [12]. After that, a ~30 nm indium-gallium-zinc oxide (IGZO) active layer with a molar ratio of In_2O_3:Ga_2O_3:ZnO = 1:1:1 was sputter-deposited. The active layer was subsequently patterned and capped with a 300 nm SiO_x etch-stop layer (ES) which was deposited in the same PECVD apparatus. Second oxidizing annealing with the same condition was employed to enhance the ES quality. After the contact holes were opened, S/D metal electrodes consisting of a stack of sputtered 300 nm aluminum on 50 nm Mo were patterned. The TFT was then “activated” again at 400 °C in an O_2 atmosphere for 2 hours to thermally-induce the highly conductive S/D regions [12]. Shown in Fig. 1 is a cross-sectional schematic diagram of the resulting TFT.

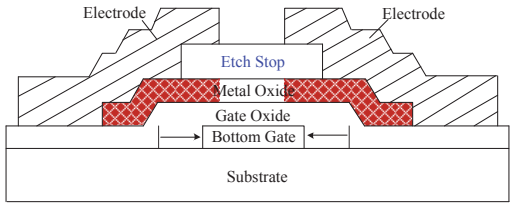

Fig. 1 Schematic diagrams of (a) the IGZO TFTs with thermally induced and highly conductive S/D regions (cross hatched)

3 RESULTS

The TFTs were subjected to positive gate-bias (V_g) and temperature (T) stresses with different V_g and T. During stress, the S/D electrodes were all grounded (V_s=V_d= 0 V) while measuring transfer characteristics, V_{ds} was fixed at 5 V. The transfer characteristics were measured in the dark immediately after each stress duration (t) by using an Agilent 4156C Semiconductor Parameter Analyzer. Here, turn-on voltage (V_{on}) is defined as the V_g at which an exponential increase in the drain current (I_d) is first observed.

It is clear from Fig. 2 that the as-fabricated TFTs exhibit a negative shift in V_{on} with a slight ΔSS after experiencing PBTS. No significant difference in the degradation was observed for TFTs with different channel width (W). As mentioned above, stress-created shallow donor-liked defects are supposed to be the major origin for the negative shift. The Arrhenius plot of $|\Delta V_{on}|$ after 10000 s PBTS with different temperature T (90, 120 and 150 °C) was drawn in Fig. 3 and an activation energy (E_A) of ~0.26 eV was obtained. A higher positive V_g and temperature T adopted in PBTS result in a larger magnitude of the shift.

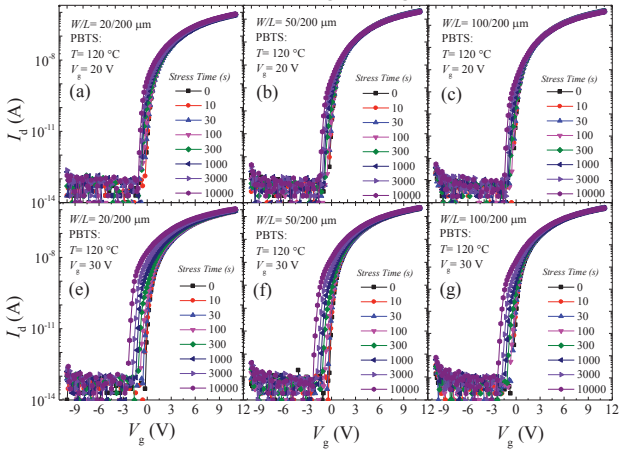

Fig. 2 The PBTS-induced time-evolution of the transfer characteristics of as fabricated IGZO TFTs with different channel width: (a-c) V_g=20 V, (d-f) V_g =30 V.

After storing in the air ambience for three months, same PBTS stress were performed on the same wafer but different devices. Except for the aggravated abnormal negative ΔV_{on}, an apparent channel-width dependence of ΔV_{on} is also found in Fig. 4 when comparing TFTs with W=100/50/20 μm. Severer shifts are observed in TFTs with a narrow channel-width. An up to ~−8 V ΔV_{on} after stressing at V_g=30 V and T=120 °C is obtained for the TFT with a W of 20 μm for 10000 s. While under the same stress condition, the ΔV_{on} is much smaller, only ~−3 V if W increases to 100 μm. Although all degradation is reduced under a weaker gate-bias (V_g=20 V), still a narrow TFT corresponds to a larger magnitude of ΔV_{on}. Furthermore, the T-dependent ln|ΔV_{on}| measured from these TFTs with different W exhibits almost the same slope in Fig. 5. A similar E_A (~0.29 eV) indicates the mechanism is identical for PBTS-induced degradation although TFTs are stored in the ambient for long-term.

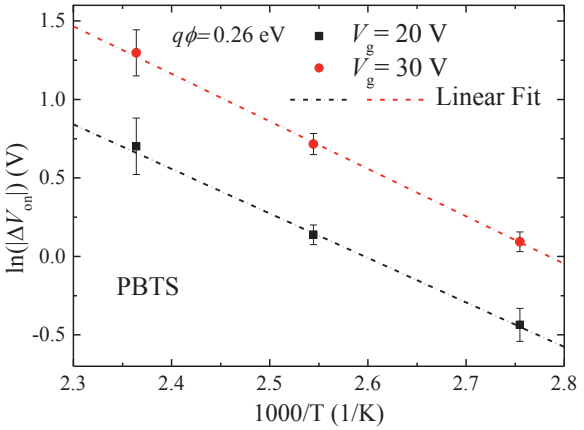

Fig. 3 The Arrhenius plot of ln(|ΔV_{on}|) on 1000/T for as fabricated IGZO TFTs subjected to PBTS at V_g= 20 V or 30 V.

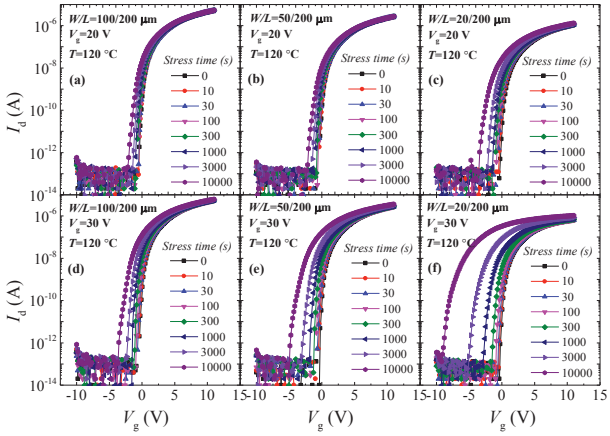

Fig. 4 The PBTS-induced time-evolution of the transfer characteristics of 3 months-stored IGZO TFTs with different channel width: (a-c) V_g=20 V, (d-f) V_g =30 V.

According to the emerging channel-width-dependent ΔV_{on}, it is supposed that most donor-liked defects are generated at the edges and diffuse across the channel, thus causing the distributed defect density is negatively related with W. As a consequence, PBTS will result in a

higher defect density within the channel in the TFTs with a smaller W and hence a corresponding more negative ΔV_{on}.

As the generation barrier for the donor-liked defects is not so high and the diffusion coefficient should be high enough for defects diffusion across the channel width, hydrogen-related hydroxyl groups (OH^-) are assumed to be the role of such shallow donor-liked defects.

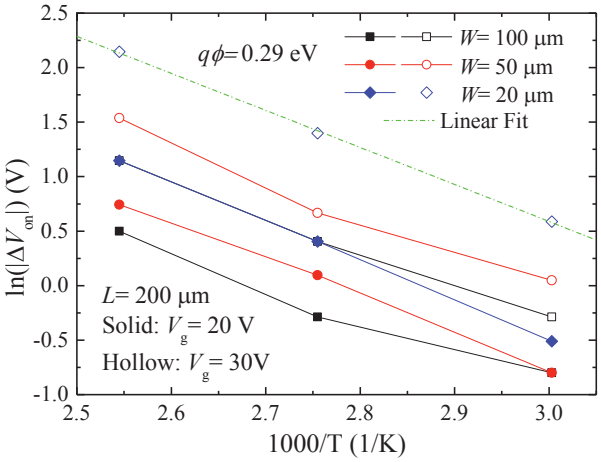

Fig. 5 The Arrhenius plot of ln(|ΔV_{on}|) on 1000/T for 3 months-stored IGZO TFTs subjected to PBTS at V_g= 20 V or 30 V.

4 CONCLUSIONS

The positive gate-bias and temperature stress (PBTS) induced degradation in an indium-gallium-zinc oxide (IGZO) thin-film transistor (TFT) has been characterized. It is found that the generation of shallow donor-like defects, assisted by thermal kinetic energy, gives rise to a negative shift of turn-on voltage (ΔV_{on}), a degraded subthreshold swing (ΔSS) in the TFTs' transfer characteristics. Severer shifts are observed in TFTs with a narrow channel-width, indicating the degradation occurs largely at the width-wise channel edges.

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REFERENCES

[1] E. Fortunato, P. Barquinha and R. Martins, "Oxide semiconductor thin-film transistors: a review of recent advances," Adv Mater, vol. 24, (22), pp. 2945-2986, 2012.

[2] J. K. Jeong, "The status and perspectives of metal oxide thin-film transistors for active matrix flexible displays," Semicond. Sci. Technol., vol. 26, no. 3, p. 34008, 2011.

[3] T. Hsieh, T. Chang, T. Chen, and M. Tsai. "Review of present reliability challenges in amorphous In-Ga-Zn-O thin film transistors." ECS Journal of Solid State Science and Technology, vol. 3, no. 9 , pp. Q3058-Q3070. 2014.

[4] D. Wang, M. P. Hung, J. Jiang, T. Toda, and M. Furuta. "Suppression of degradation induced by negative gate bias and illumination stress in amorphous InGaZnO thin-film transistors by applying negative drain bias." ACS applied materials & interfaces, vol. 6, no. 8 , pp. 5713-5718. 2014.

[5] J. G. Um, M. Mativenga, P. Migliorato, and J. Jang. "Defect generation in amorphous-indium-gallium-zinc-oxide thin-film transistors by positive bias stress at elevated temperature." J. Appl. Phys., vol. 115, no. 13 , pp. 134502. 2014.

[6] J. Rhee, S. Choi, H. Kang, J. Kim, D. Ko, G. Ahn, H. Jung, S. Choi, D. M. Kim, and D. H. Kim. "The electron trap parameter extraction-based investigation of the relationship between charge trapping and activation energy in IGZO TFTs under positive bias temperature stress." Solid-State Electronics, vol. 140, pp. 90-95. 2018.

[7] S. Jin, T. Kim, Y. Seol, M. Mativenga, and J. Jang. "Reduction of positive-bias-stress effects in bulk-accumulation amorphous-InGaZnO TFTs." IEEE Electron Device Lett., vol. 35, no. 5 , pp. 560-562. 2014.

[8] S. Huang, T. Chang, M. Chen, S. Chen, C. Tsai, M. Hung, C. Tu, C. Chen, J. Chang, and W. Liau. "Effects of ambient atmosphere on electrical characteristics of Al2O3 passivated InGaZnO thin film transistors during positive-bias-temperature-stress operation." Electrochemical and Solid-State Letters, vol. 14, no. 4 , pp. H177-H179. 2011.

[9] T. Toda, G. Tatsuoka, Y. Magari, and M. Furuta. "High-performance top-gate and self-aligned In–Ga–Zn-O thin-film transistor using coatable organic insulators fabricated at 150° C." IEEE Electron Device Lett., vol. 37, no. 8 , pp. 1006-1009. 2016.

[10] C. Tu, W. Lin, C. Chen, M. Hung, J. Chang, M. Chiang, and W. Liao, "P ‐ 15: Bias Stress Reliability for w/and w/o Oxide ‐ passivated IGZO TFTs," in SID Symposium Digest of Technical Papers: Wiley Online Library2011, pp. 1151-1153.

[11] H. Im, H. Song, J. Jeong, Y. Hong, and Y. Hong. "Effects of defect creation on bidirectional behavior with hump characteristics of InGaZnO TFTs under bias and thermal stress." Japanese Journal of Applied Physics, vol. 54, no. 3S , pp. 03CB03. 2015.

[12] L. Lu, J. Li, H. S. Kwok, and M. Wong, "High-performance and reliable elevated-metal metal-oxide thin-film transistor for high-resolution displays," in 2016 IEEE International Electron Devices Meeting (IEDM), pp. 32.2. -32.2.4.