Stable and High-mobility Oxide TFTs using Low-temperature Processed ZTO/IZO Stacked Channels

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ABSTRACT

We fabricated Zn-Sn-O (ZTO)-based oxide and In-Zn-O (IZO) stacked channel thin-film transistors (TFTs) by experimentally using ultraviolet (UV) annealing for activation. The field-effect mobility was about 30 cm^2/Vs, and the threshold voltage (V_{th}) was–3.5 V at the UV annealing temperature of 200°C. These TFTs improved the reliability of the negative gate bias illumination stress (NBIS) test more than the In-Ga-Zn-O (IGZO) TFTs did. The ZTO/IZO stacked channel TFTs are promising candidates for next-generation flexible devices.

1 INTRODUCTION

Oxide thin-film transistors (TFTs) are the key devices for ultra-high resolution liquid crystal displays (LCDs) and organic light emitting diode (OLED) displays. The oxide semiconductor materials that make up TFTs can be deposited by a sputtering method, and large-area fabrication at a low cost is possible. One of the representative oxide TFTs is an amorphous In-Ga-Zn-O (a-IGZO) TFT [1, 2]. The a-IGZO TFTs have excellent characteristics including high mobility (typically > 10 cm^2/Vs) and a low off-current compared with amorphous Si (a-Si) TFTs. However, a-IGZO TFTs are not available for flexible device application because they require high-temperature activation of at least 350°C, which exceeds the required process temperatures for flexible device fabrication (< 200°C) [3]. The process temperature and properties of each TFT material are listed in Table 1. For this requirement, we used the stacked structure of a Zn-Sn-O (ZTO)-based oxide as a layer with carrier control and In-Zn-O (IZO) as a layer with high carrier density [4]. ZTO-based oxide has superior carrier control, as we already reported [5]: namely, a mobility of 50 cm^2/Vs in ZTO-based oxide and ITO stacked channel TFTs by a room temperature process. However, stacked TFTs have a problem: there is a V_{th} negative shift during a subsequent high-temperature process. In the present study, we have developed high-mobility stacked channel TFTs with stable and controllable V_{th} by using a low-temperature ultraviolet (UV) annealing method.

2 EXPERIMENT

2.1 Experimental Method

We used back-channel-etch (BCE)-type TFTs, as shown in Figs. 1 and 2. The process flow is detailed in Table 2. The substrates were made of a SiO_2 (140 nm) layer on a Si substrate (n type, resistivity < 0.007 Ωcm), which was used as a gate electrode. The stacked channel of the ZTO-based oxide (15–30 nm) layer and the IZO or ITO (5 nm) layer was deposited by a DC sputtering method at room temperature. The ZTO-based oxide is an OS-Z series sputtering target manufactured by Hitachi Metals, Ltd. The OS-Z oxide annealing can be done at low temperature, around 200°C. The channel was formed by photolithography and a wet etching process. The stacked channel was activated by thermal annealing at 150–350°C for 1 h under atmospheric air or ultraviolet (UV) annealing [3, 4]. The UV lamp had a center wavelength of 254 nm and a power density of 40 mw/cm^2. Source and drain (S/D) electrodes were Mo (140 nm) deposited by DC sputtering at room temperature and formed by photolithography and the wet etching process (L = 10 um, W = 100 um). These TFTs were fabricated without a passivation film.

2.2 Reliability Measurement Method

A positive gate bias stress (PBS) test and a negative gate bias illumination stress (NBIS) test were performed on the TFTs. A gate voltage (V_g) of 15 V for a total stress time of 1000 s was applied for PBS. A V_g of –15 V with a tungsten lamp of 1000 lx for a total stress time of 1000 s was applied for NBIS. PBS and NBIS tests were evaluated in a dry condition atmosphere.

3 RESULTS

Figure 3 shows the transfer characteristics of ZTO-based oxide and IZO or ITO stacked channel TFTs. The annealing temperature was 300°C at the hot plate. As shown in the figure, ZTO/ITO stacked channel TFTs exhibited large V_{th} negative shifts, but those of the ZTO/IZO stacked channel TFTs were relatively low. This is because ITO transformed from an amorphous phase to a crystalized form during 300°C annealing, which changed the carrier condition. On the other hand, IZO maintained an amorphous form and the same carrier condition as before annealing. Figure 4 shows the dependence of the mobility and V_{th} on the annealing temperature. In order to keep V_{th} small (around 0 V), the annealing temperature should be around 200°C. However, to achieve field effect mobility > 30 cm^2/Vs, the annealing temperature should be more than 250°C. To overcome this trade-off, we applied UV annealing, which is effective for the stable operation of oxide TFTs for the

activation [6, 7]. The TFTs with the UV annealing at 200°C showed V_{th} of –3.5 V and a mobility of 29.5 cm^2/Vs, while the conventional hot plate annealing showed a low mobility of 16.1 cm^2/Vs along with a hump in the transfer characteristics, as shown in Fig. 5. This result demonstrates that UV annealing is preferable for the low-temperature process on the stacked channel oxide TFTs. We also found that the developed stacked channel oxide TFTs improved the reliability compared with the ZTO-based oxide TFTs and the conventional IGZO TFTs, as shown in Figs. 6 and 7. We conclude that the ZTO-based oxide in the stacked channel has an excellent V_{th} controllability, and that the V_{th} shift was suppressed compared with the single layer oxides.

4 CONCLUSION

We developed ZTO-based oxide and IZO stacked channel TFTs with a low-temperature process using UV annealing (200°C). The field-effect mobility was about 30 cm^2/Vs, and V_{th} was –3.5 V. The ZTO-based oxide and IZO stacked channel TFTs improved the reliability of the NBIS test more than the ZTO-based oxide TFTs and IGZO TFTs did. These results demonstrate that the TFTs are promising candidates for next-generation flexible devices.

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Table 1 Properties of TFT materials.

	a-Si	LTPS	a-IGZO	ZTO/ITO stacked
Large aria process	Available	Not available	Good	Good
Process temperature [°C]	<350	600	350<	RT
Mobility [cm^2/Vs]	0.5-1.5	100	10	50

Table 2 Process flow of TFTs.

No	Process step	Parameters
1	Gate Insulator (Furnace)	SiO_2 = 140 nm Temp: 900°C
2	Channel 1 (Sputtering)	IZO = 5 nm Temp = RT
3	Channel 2 (Sputtering)	ZTO = 15 - 25 nm Temp: RT
4	Patterning (Wet Etching)	Oxalic acid based Temp: RT
5	Activation (Hot plate or UV)	Temp: 200 - 350°C Time : 60 min UV: 40 mW/cm^2
6	S/D Electrodes (Sputtering)	Mo = 140 nm Temp: RT
7	Patterning (Wet Etching)	Phosphoric-Acetic-Nitric acid based Temp: RT
8	Activation (Hot plate)	Temp: 130°C Time: 60 min

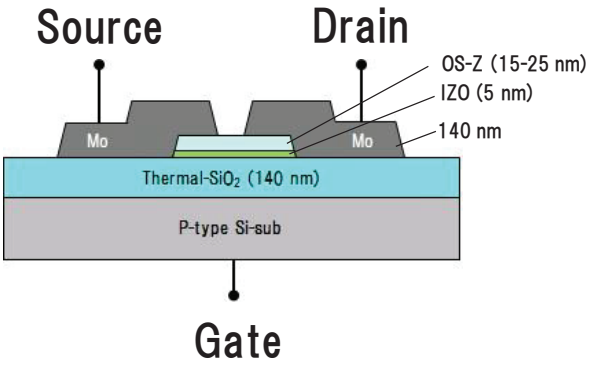

Fig. 1 Schematic cross-section of BCE TFTs.

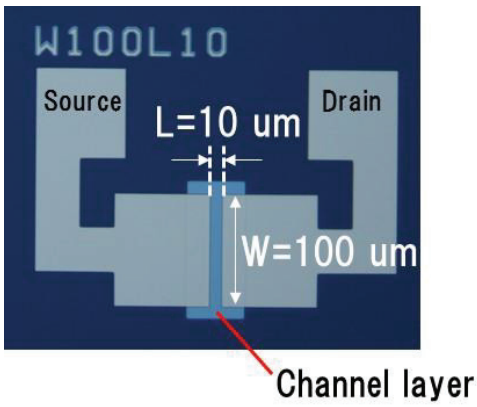

Fig. 2 Schematic top view of BCE TETs.

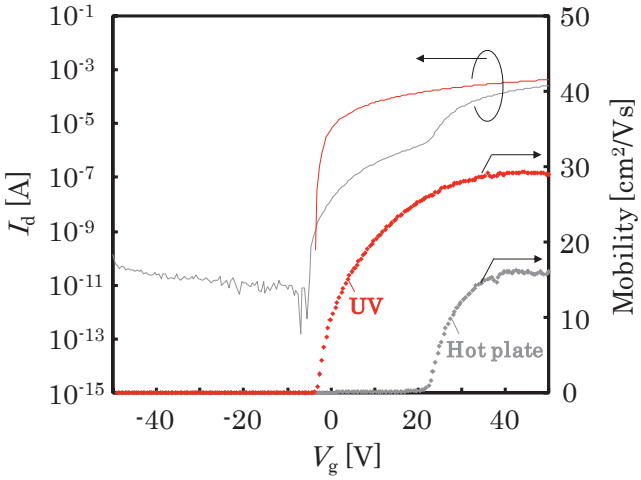

Fig. 5 Comparison of transfer characteristics of TFTs by difference in annealing method (200°C).

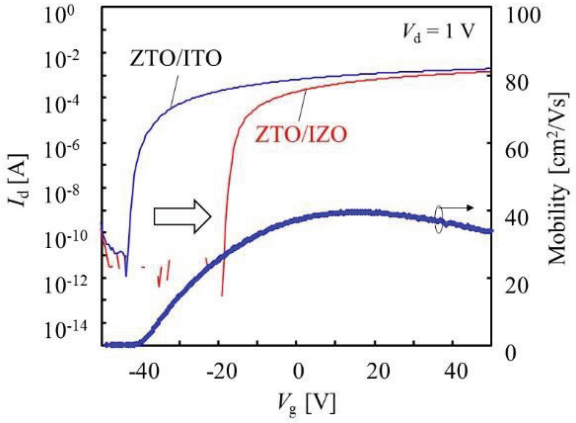

Fig. 3 Transfer characteristics of stacked channel TFTs (hot plate annealing 300°C).

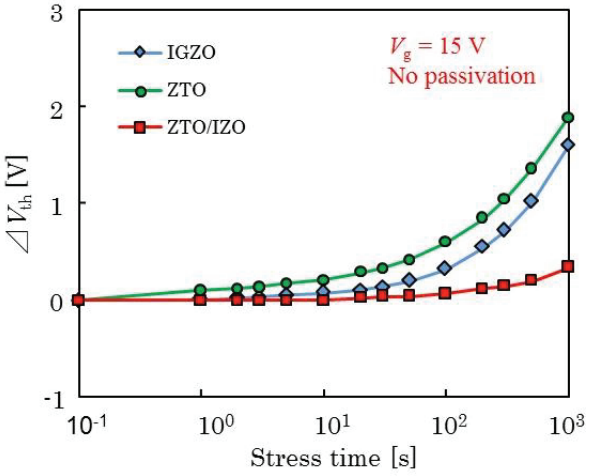

Fig. 6 Reliability of TFTs (PBS).

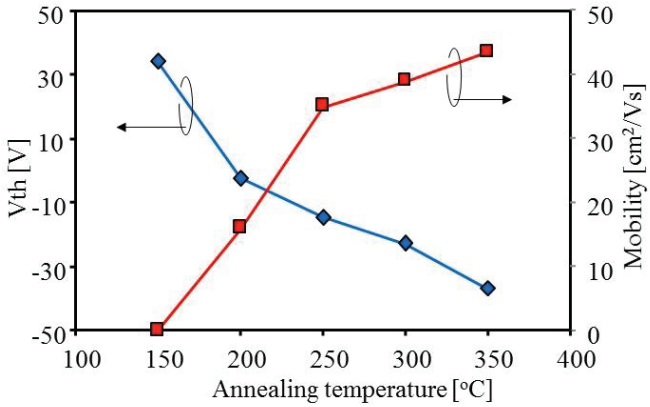

Fig. 4 Annealing temperature dependence of V_{th} and field-effect mobility (ZTO/IZO stacked channel TFTs).

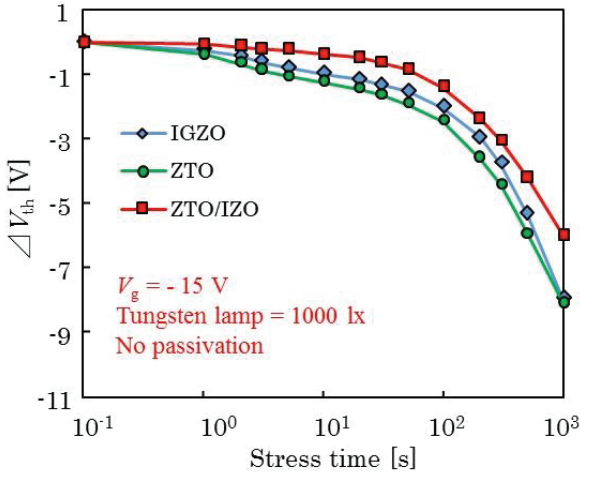

Fig. 7 Reliability of TFTs (NBIS).