E/E Inverter Using Four-Terminal Poly-Ge_xSn_{1-x} TFTs on Glass

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Keywords: TFT, 4T, Poly-GeSn, Cu-MIC, E/E inverter

ABSTRACT

We demonstrated an E/E inverter using polycrystalline germanium-tin (poly-Ge_xSn_{1-x}) thin-film transistors (TFTs) fabricated via metal-induced crystallization (MIC) using Cu. The TFTs in the E/E inverter comprises a planar four-terminal (4T) structure, in which the TFTs were enabled to be normally-off by the control gate voltage (V_{CG}). The inverter performance was varied by changing V_{CG}.

1 INTRODUCTION

Ge is expected as a next-generation channel material because of its high carrier mobility [1, 2]. Recently, germanium-tin (Ge_xSn_{1-x}) has also attracted attention because the mobility of Ge_xSn_{1-x} is enhanced comparison with Ge [3]. Incorporating Sn (more 6.5%) over the solubility limit changes the band structure from an indirect-gap one to a direct-gap one [4, 5]. Therefore, Ge_xSn_{1-x} is expected to be used as materials for optoelectronic devices such as lasers and LEDs. In addition, it is expected as a channel material for metal–oxide–semiconductor field-effect transistors (MOSFETs) [6-11].

In addition to MOSFET, polycrystalline Ge_xSn_{1-x} (poly-Ge_xSn_{1-x}) thin film is expected as a candidate material for thin-film transistors (TFTs). Recently, several researches reported high hole mobility of poly-Ge_xSn_{1-x} thin films on insulators [12-14]. In general, Ge-based polycrystalline thin-film materials with < 50-nm thickness generate high hole concentration of 10^{18} cm^{-3}. Even if a pseudo-single-crystalline Ge-based film was grown using a thick initial film, the hole concentration approaches 2×10^{17} cm^{-3}. This high concentration makes it difficult to form junctionless (JL) p-ch TFTs. If Ge and Ge_xSn_{1-x} are thick under the solid-phase crystallization (SPC) process, the chemical mechanical polish (CMP) thinning process is required to fully deplete the TFTs, as reported in Ref. [15, 16].

We demonstrated double-gate (DG) and four-terminal (4T) poly-Ge and poly-Ge_xSn_{1-x} TFTs by using the Ge and Ge_xSn_{1-x} film with thickness less than 25 nm and Cu metal-induced crystallization (Cu-MIC) on a glass and flexible plastic substrate [17-22]. In the 4T structure, the top gate (TG) and bottom gate (BG) operate independently and are used as drive and control gate or vice versa. This enable us to vary the threshold voltage (V_{th}) of the TFT [23, 24] and to form an E/E inverter. In this research, we fabricated fully depleted 4T poly-Ge_xSn_{1-x} TFTs on a glass substrate and applied them to an E/E inverter.

2 EXPERIMENT

2.1 4T Cu-MIC poly-Ge_xSn_{1-x} TFT

The channel layer is deposited by a multi-target sputtering system using Ar gas without a heating glass substrate. Three layers in the order of Ge_xSn_{1-x}/Cu/Ge_xSn_{1-x} were deposited, without breaking vacuum. In this experiment, we used the Ge_xSn_{1-x} target with a Sn concentration of 7%. Figure 1 shows the Raman spectrum of the Cu-MIC poly-Ge_xSn_{1-x} thin film and SPC poly-Ge_xSn_{1-x} thin film without Cu, which were crystallized at 500 ℃ for 5 h in N_2 gas. The peak intensity of Cu-MIC is larger than that obtained using the SPC process. Furthermore, the full width of half maximum

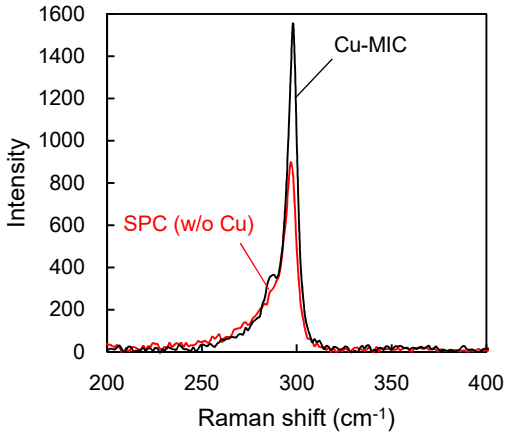

Fig. 1. Raman spectrum of poly-Ge_xSn_{1-x}

(FWHM) was estimated to be 6.1 cm^{-1} and 8.1 cm^{-1} for Cu-MIC and SPC, respectively. This result indicates that the amorphous phase of Cu-MIC is smaller than that obtained using the SPC process and the quality of Cu-MIC is superior to that of the SPC process. When the hole density of the channel layer is 2×10^{18} cm^{-3}, the maximum depletion layer is approximately 15 nm. If the thickness of the channel layer is larger than 15 nm, it will be a normally-on TFT because fully depletion will not be completed owing to the large leakage current. In this case, it could not be used for an E/E inverter. To overcome this issue, the thickness of the channel layer in this experiment was adjusted to be 15 nm by tuning the sputtering duration.

The process flow and cross-section of the TFT are shown in Fig. 2. The bottom-gate (BG) and top-gate (TG) metals are composed of Mo. The BG dielectric was made up of two layers. First, hafnium dioxide (HfO_2) was

deposited by reactive sputtering; subsequently, 5.0-nm silicon dioxide (SiO_2) was deposited by plasma-enhanced chemical vapor deposition (PECVD). The TG dielectric SiO_2 with a thickness of 30 nm was deposited by PECVD. The equivalent oxide thickness (EOT) of the BG dielectric is half of that of the TG dielectric. Cu-MIC in the TFT fabrication process was carried out at 500 ℃ for 10 h in N_2 gas. An aluminum lateral metal source drain (AL-LM-SD) was formed by final annealing to reduce parasitic resistance of SD [17]. Figure 3 shows the photograph of the TFT fabricated in this research. The gate length and width are 20 μm and 10 μm, respectively.

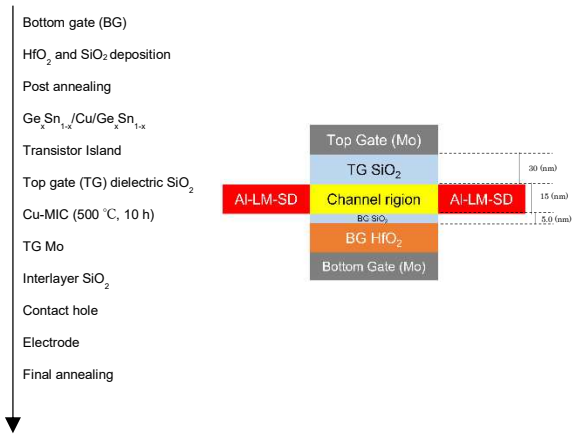

Fig. 2. Process flow and cross sectional of TFT

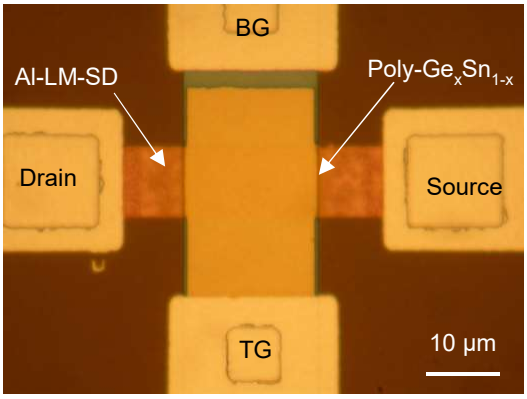

Fig. 3. Photograph of TFT

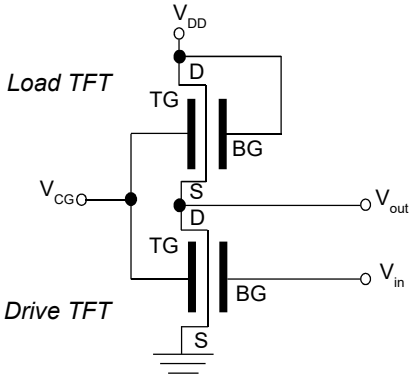

Fig. 4. E/E inverter circuit diagram in this research

2.2 E/E inverter

The E/E inverter composed of 4T TFTs is shown in Fig. 4. In this experiment, the BG and TG were used as the drive and control gate, respectively. The performance of the E/E inverter was investigated by changing V_{CG}.

3 RESULTS AND DISCUSSION

3.1 4T Cu-MIC poly-Ge_xSn_{1-x} TFT

Figures 5 and 6 show the transfer characteristic, when the BG and TG was used as the drive and control gate, respectively. The red bold line in Figs. 5 and 6 represent the transfer performance of the DG, which is connecting

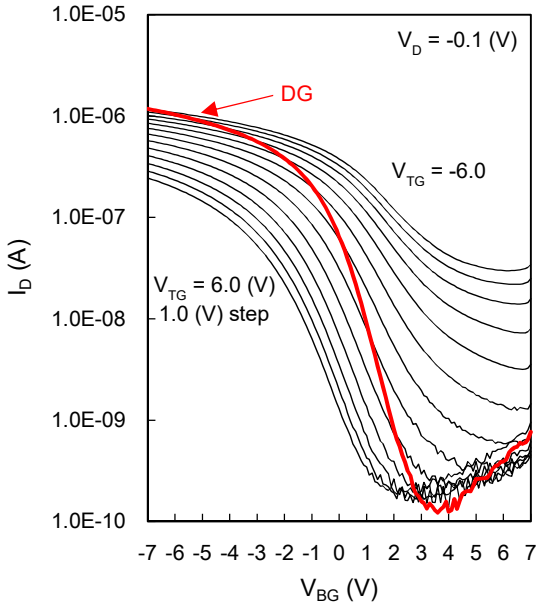

Fig. 5. Transfer characteristics (BG drive)

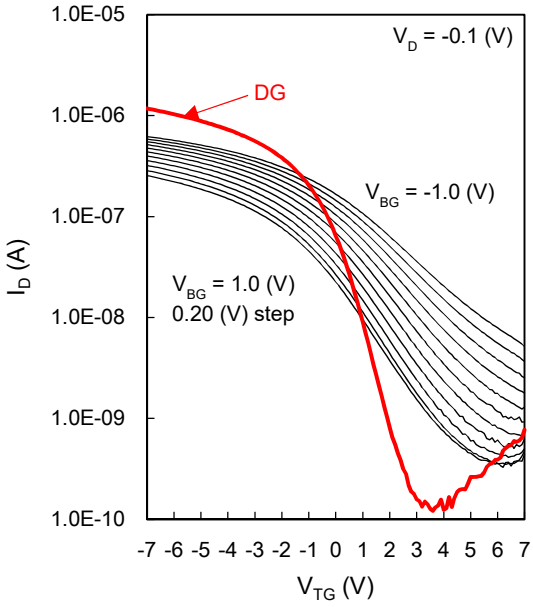

Fig. 6. Transfer characteristics (TG drive)

the BG and TG. The I_{on}/I_{off} of the DG is approximately 7500, and s.s. is approximately 0.85 V/dec. This DG performance was significantly improved as compared with that of our previous work [22] because the thickness of the channel layer was decreased. This improvement leads to fully depletion, namely low leakage current.

The controllability of V_{th} is summarized in Fig. 7. With increasing V_{CG}, V_{th} decreases. The measurement range of V_{CG} is different between the BG drive and TG drive because of the strong V_{th} variation for the TG drive compared to that of the BG drive. If γ is defined as $|\Delta V_{th}/\Delta V_{CG}|$, γ in the BG ($\gamma_{BG}$) and TG ($\gamma_{TG}$) drive are 0.44 and 1.43, respectively. The difference in magnitude of γ is caused by the difference in EOT between the BG and the TG [23, 24].

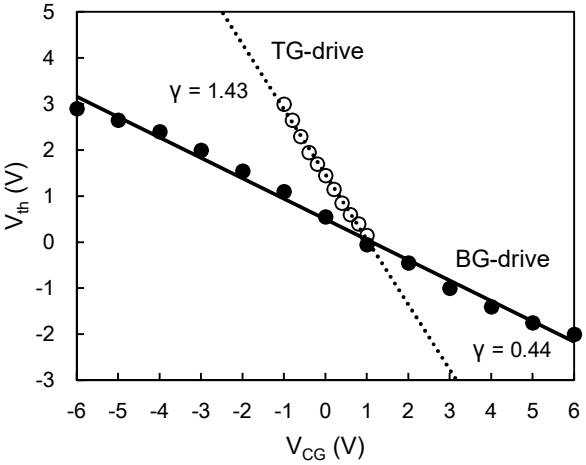

Fig. 7. Controllability of V_{th}

3.2 E/E inverter

The performance of the E/E inverter made up of a 4T Cu-MIC poly-Ge_xSn_{1-x} TFT is shown in Fig. 8. V_{in} was varied from 0 V to -5.0 V for a V_{DD} of -5.0 V. V_{CG} was applied from 1.5 V to 4.5 V with steps of 1.0 V. The inverter characteristic is superior with increasing V_{CG}. This is caused by negative V_{th} shift with increasing V_{CG}, as shown in Fig. 7. This indicates successful enhancement operation of the 4T TFTs in E/E inverter. However, the gain ($\Delta V_{Out}/\Delta V_{In}$) is less than 1.0 and the logic swing value is significantly less than V_{DD}. One solution to improve performance is to apply an E/D inverter. The 4T TFTs enable us to form an E/D inverter by adjusting V_{CG}.

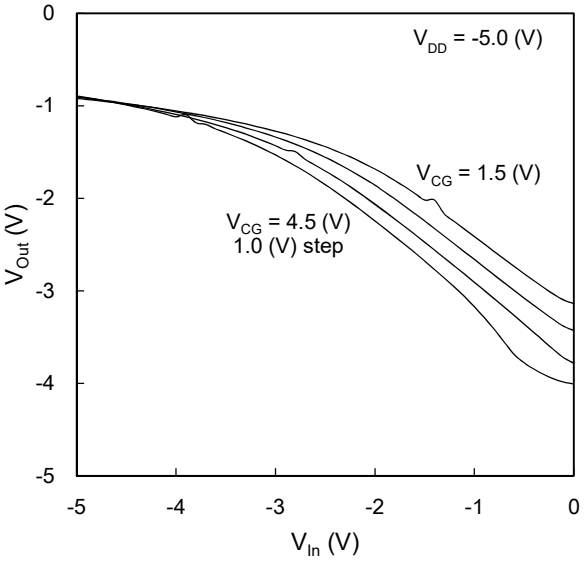

Fig. 8. Performance of E/E inverter changing V_{CG}

4 CONCLUSIONS

The E/E inverter using Cu-MIC 4T poly-Ge_xSn_{1-x} TFTs was successfully demonstrated using two key technologies. First, the 4T TFTs were used for the inverter to adjust V_{th}. Second, the thin Cu-MIC poly-Ge_xSn_{1-x} film (<20 nm) was applied to complete fully depletion.

ACKNOWLEDGMENTS

This study was supported in part by the Japan Society for the Promotion of Science through Grants-in-Aid for Scientific Research (C) 16K06311 and (C) 19K04534. A part of this work was supported by IKETANI SCIENCE AND TECHNOLOGY FUNDATION.

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