P-type LTPS Gate Driver to Generate Simultaneous and Overlapping Progressive Outputs for High-Resolution AMOLED Displays

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ABSTRACT

A new low-temperature polycrystalline silicon (LTPS) gate driver is developed for active-matrix organic light-emitting diode (AMOLED) pixel circuits using simultaneous-emission (SE) driving scheme. Simulated results indicate that the proposed circuit successfully generates waveforms within the rising time of 0.6 μs under the RC loadings of 9.96 kΩ and 21.2 pF.

1 INTRODUCTION

Integrating gate driver circuit on glass substrate brings a lot of benefits, including low cost and overall compactness, so such technique has become a mainstream in industry [1]-[6]. Additionally, to pursue clear and vivid visual experience, high-resolution and high-frame-rate panels are required with high-speed-driving gate driver circuits [4]-[6]. Low-temperature poly-silicon thin-film transistors (LTPS TFTs) is more potential than amorphous silicon (a-Si:H) TFTs because LTPS TFTs have better driving capability and short response time. Thus, the size of LTPS TFTs can be designed smaller than that of a-Si TFTs for generating the output waveforms based on the same specification of panels, leading to a small layout area of LTPS gate driver circuits. Moreover, the parasitic capacitance is large in a-Si:H TFTs, increasing the instability factors of gate driver circuits and causing fluctuations of outputs. Also, a-Si:H TFTs have a degradation problem under stress, so the rising time or falling time of the output signals may become longer after long-term operation, resulting in poor image quality. In spite of the above-mentioned advantages of LTPS TFTs, the resistor-capacitor (RC) loading of row lines is still a big issue. In the progressive emission (PE) mode driving scheme, high-resolution panels require a short scan time for each row. Thus, pixel circuits may not be able to receive precise data voltage and finish complete compensation because of insufficient time. The RC loadings in row lines further distort the output pulses of gate driver circuits, resulting in higher error rates of the pixel circuits. To overcome this problem, several studies proposed the gate driver which can generate overlapping outputs. Lin et al. [5] proposed a simplified gate driver circuit with three-phase overlapping clock signals to realize overlapping outputs for being used in high-resolution and narrow-bezel applications. Also, a gate driver circuit using a two-step-boosting structure to generate high slew rate and overlapping outputs for high-resolution and high-frame-rate displays is developed [6]. The overlapping outputs of gate driver circuits expand the pulse width for driving pixels, so two rows of pixel circuits can operate in the same period, retarding the effect of RC loadings. For pursuing higher resolution displays, the simultaneous emission (SE) mode driving scheme tends to be a better way owing to longer compensation period than PE driving scheme. Since the RC loadings are inevitable and increases as the resolution becomes higher, the gate driver circuits with overlapping outputs for the data input period of SE driving scheme is needed.
This work proposes a p-type LTPS gate driver circuit with two inverted clocks and two controlling signals to generate two kinds of output signals for the SE driving scheme. By using the coupling effect from the RC loading of the row line, no extra voltage level is needed in the proposed circuit. Based on simulated results of the eight-stage proposed gate driver circuit, simultaneous and overlapping progressive signals for a 5.15-inch 240 Hz FHD display are successfully generated and the rising time of waveforms is within 0.6 μs.

2 EXPERIMENT

Fig. 1 presents the schematic of the proposed gate driver circuit and the relevant timing diagram. The circuit is composed of 13 p-type LTPS TFTs and two capacitors. C1 is used to bootstrap the Q[N] node for driving TFT (T4) to generate overlapping progressive waveforms. C2 is used for coupling voltage to S[N] node from a row line to fully turn on T5 and generate a simultaneous waveform. Two clock signals (CK and XCK) and two constant voltage powers (VGH and VGL) are used to drive the circuit. Besides, two control signals (SS and SR) are required for generating simultaneous outputs. Fig. 2 shows the block diagram of the proposed gate driver circuit. OUT[N] is the output node of the [N]th stage and used for resetting the [N-2]th stage. The circuit operation can be divided into eight periods and described as follows.

![Block diagram of proposed gate driver circuits.](image)

**Fig. 2 Block diagram of proposed gate driver circuits.**

In the first period, SS is at high and SR is at low. When CK goes to VGL, the P[N] node is discharged to VGL + ΔV2 and turns on T10, T11 and T13. Therefore, the Q[N] and OUT[N] nodes are stabilized at VGH. During the second period, SS turns to VGL and SR turns to VGH. The S[N] node is discharged to a low voltage for turning on T5 and the OUT[N] node starts discharging. Since the OUT[N] node connects to the whole [N]th row, the RC loadings of the row line causes the OUT[N] node to be discharged slower than the S[N] node. As the S[N] node is discharged to VGL + |VTH_T6|, T6 is turned off automatically and T5 is still turned on for discharging the OUT[N] node. Thus, S[N] node becomes floating and is coupled to VGL - ΔV. Therefore, T5 is at the linear region, and the OUT[N] node is able to reach VGL. At the same time, T9 which is designed to be larger than T7 is turned on, and the P[N] node is kept at a high voltage to turn off T11 and T13 for a stable output. Next, in the third period, SS is turned back to VGH and SR is turned back to VGL. T12 is turned on for keeping the S[N] node at VGH, and T5, T6 and T9 are turned off. When CK goes to VGL, the P[N] node is discharged to VGL + [VTH_T6] through T7. Therefore, T10, T11 and T13 are turned on to stabilize the Q[N] and OUT[N] nodes at VGH. In the fourth period, the Q[N-1] signal from the previous stage changes to low. The Q[N] node is discharged to VGL + [VTH_T5] through T12. Therefore, T4 is turned on for discharging the OUT[N] node and the overlapping output is realized. In addition, T8 is designed to be larger than T7, so the P[N] node is charged at a high voltage of VGH - ΔV2 even though T7 is turned on. Therefore, T10, T11 and T13 are turned off so that the Q[N] and OUT[N] nodes are prevented from being charged. In the fifth period, XCK changes from high to low. Since the Q[N-1] Signal changes to VGL, the Q[N] node becomes floating and is coupled to a lower voltage of VGL + [VTH_T1] - ΔV1. Therefore, T4 can be operated at the linear region and VGL is completely transmitted to the OUT[N] node. Additionally, T8 is turned on to stabilize the Q[N] node.
on, and CK changes to high so that P[N] node is charged to VGH. T10, T11 and T13 are turned off to prevent the OUT[N] node from being charged. In the sixth period, XCK turns back to VGH and the OUT[N+2] signal from next two stage becomes low. Thus, the Q[N] node is charged through T3 for turning off T4. Meanwhile, CK changes to VGL and the P[N] node is discharged to VGL + |VTH_T7|. Therefore, T10, T11 and T13 are turned on for charging the Q[N] and OUT[N] nodes. In the seventh period, the OUT[N+2] node is still at VGL and the Q[N] node is kept at VGH for turning off T4. The P[N] node remains at VGL + |VTH_T7| because there is no charging path for the P[N] node. Thus, T10, T11 and T13 are turned on for charging the Q[N] and OUT[N] nodes. In the eighth period, the OUT[N+2] signal changes to VGL, and T3 is turned off. The P[N] node is periodically set to VGL + |VTH_T7| as CK changes to VGL, stabilizing the Q[N] and OUT[N] nodes at VGH.

3 RESULTS

To verify the functionality of the proposed gate driver circuit, HSPICE simulator and a p-type LTPS TFT model are used. Table I lists the designed parameters, including the voltage swings of clock signals (CK and XCK) and controlling signals (SS and SR), the voltage levels of constant power signals (VGH and VGL), and the size of each TFT (T1-T13). To meet the requirements of 5.15-inch 240 Hz Full HD (1080×1920) panels, the pulse width of CK and XCK is set to 2\,\mu s, and the RC loadings in row lines are set to 9.96 k\,\Omega and 21.2 pF.

Fig. 3 plots the simulated waveforms of clock signals, control signals, Q[N-1], Q[N], OUT[N-1], OUT[N], OUT[N+2], P[N], and S[N]. As shown in Fig. 3, OUT[N-1], OUT[N] and OUT[N+2] simultaneously output -8 V to the row lines. At the same time, P[N] and Q[N] are at about 8 V to prevent OUT[N] from being charged. As SS changes to 8 V and SR changes to -8 V, P[N] decreases to about -1.2 V and OUT[N] can be raised up to 8 V. When Q[N] is coupled to -16.1 V, Q[N] node is discharged to -5.23 V. Thus, T4 is turned on and starts discharging OUT[N]. Next, XCK turns from 8 V high to -8 V, and Q[N] is coupled to -16.1 V. Therefore, T4 is operated at the linear region and OUT[N] can be discharged to -8 V. Additionally, P[N] is kept at higher than 6.41 V for turning off the pull-up circuit when OUT[N] is discharged to -8 V. Lastly, when the reset signal OUT[N+2] from the [N+2]th stage changes to -8 V, Q[N] and OUT[N] are raised up to 8 V and remained at 8 V until both SS and SR change state again in the next frame. Fig. 4 demonstrates the simulated output waveforms of continuous eight stages. As the pixel array is operated during the compensation period, OUT[1] to OUT[8] are simultaneously discharged to -8 V for about 18\,\mu s. Afterward, OUT[1] to OUT[8] are sequentially generated for the data-input period of the pixel array. The pulse width of overlapping outputs are about 4\,\mu s for pixels to receive data voltage, able to fulfill pre-charge function for 240 Hz FHD panels. Table II shows the rising and falling times of OUT[6]. The rising times for both the compensation period and the data-input period are less than 0.6\,\mu s, ensuring the effectiveness of the proposed gate driver circuit.
4 CONCLUSIONS

In this work, a p-type LTPS gate driver circuit is proposed for driving SE mode AMOLED pixel circuits. By utilizing the coupling effect from the row lines, the simultaneous outputs are able to be discharged to VGL without additional low voltage level. Furthermore, two inverted clock signals and a storage capacitor is designed for overlapping progressive outputs, so pixels in panels can achieve pre-charging function for the accurate data voltage in high-resolution panels. Simulated results show that eight-stage gate driver circuit successfully generates the output waveforms within the rising time 0.6 μs, confirmed its effectiveness for use in 5.15-inch 240 Hz FHD displays.

CONCLUSIONS

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