Polysilicon CMOS TFTs on Ultrathin and Flexible Stainless Steel Substrates

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ABSTRACT

CMOS polysilicon TFTs fabricated on flexible stainless steel substrates are thinned down to 5 μm thickness. Bending tests show minimal change in TFT performance at 2.5 mm bending radius after 10,000 tensile bend cycles.

1 INTRODUCTION

In recent years, flexible electronics have established a key role in novel electronic applications, ranging from wearables to displays, and from solar cells to batteries. For electronic devices fabricated directly on top of flexible substrates, manufacturing processes must be compatible with the substrate type.

Flexible stainless steel substrates have significant advantages over other flexible polymer and glass substrates. Higher thermal budgets afforded by steel allows for greater flexibility in fabrication processing and improved material quality. In addition, steel offers increased dimensional stability, chemical resistance, durability, robustness, and non-permeability to water and oxygen [1]. Flexible steel is also amenable to roll-to-roll manufacturing [2], attractive for large-area, high throughput, low-cost/area applications. [3]

Applications that require low bending radii and reliability over many bending cycles have become increasingly important for display and sensor applications and are therefore extensively studied [4-6]. Polysilicon TFTs on flexible steel allows for a combination of flexibility, durability, and robustness compared to thinned silicon or glass substrates. The bending capability and reliability of devices on steel can be tuned with the choice of substrate thickness and thinning.

Here we present the dynamic bending analyses of TFTs built on flexible stainless steel substrates with a substrate thickness reduced to 5 μm. The change in TFT performance up to 10,000 cycles of 2.5R (R is the bending radius in mm) is evaluated.

By being able to apply stainless steel substrates for applications that require extreme flexibility and reliability, we can apply higher electronic device performance to the flexible electronics industry, for applications including, flexible/bendable display, flexible sensors, MEMS, and also ultrathin applications such as secure documentation and banknotes

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2 EXPERIMENT

CMOS poly-Si TFTs are fabricated on 100 μm thick, flexible, 300 x 300 mm^2 stainless-steel substrates. The bare stainless steel surface is polished to a RMS roughness of < 2 nm and has a flatness < 20 μm across the entire sheet. Complete dielectric encapsulation with a diffusion barrier is deposited to prevent metal diffusion into the polysilicon active channel or gate-oxide during subsequent high temperature steps (>800 °C). On top of this barrier and dielectric encapsulation layers, the electronic devices are fabricated. Fig. 1a shows an SEM cross-section image of a device on stainless steel, where the barrier layer can be observed. Amorphous silicon is deposited, laser-crystallized, and patterned to form the semiconductor channel. A gate-oxide is then deposited on top. A high temperature gate metal is used in conjunction with in-house proprietary printed dopant inks [7] to fabricate top-gate self-aligned polysilicon TFT devices. After the gate formation, the n- and p-type dopant materials are screen printed and cured. High temperature drive-in and activation is performed in separate steps, forming the TFT source and drain. To complete the TFT, an interlayer dielectric is deposited, after which vias are created in this layer and a contact metal is formed. The TFT schematic is shown in Fig. 1b.

Results reported here have nominal W/L transistor dimensions of 8/4 μm in all cases. Using this process scheme, Near-Field Communication (NFC) circuits operating at 13.56 MHz are enabled on large-area durable substrates that are thin, mechanically robust, and flexible (Fig. 1c). For 100 μm thick substrates, devices can withstand multiple bends at 7.5R (effective strain of 0.67 %), and show unchanged functionality when tested around a curved surface of similar radius.

To reduce the minimum bending radius, the stainless steel substrate is thinned after formation of the devices. A protective film is applied to the front surface. The barrier layer on the backside of the substrate is then removed with mechanical polish. The substrate is then thinned to a final thickness of 5 μm by wet chemical etching in ferric chloride ($FeCl_3$) for a few minutes. The topside barrier is removed for subsequent device testing. The result is shown in Fig. 2.

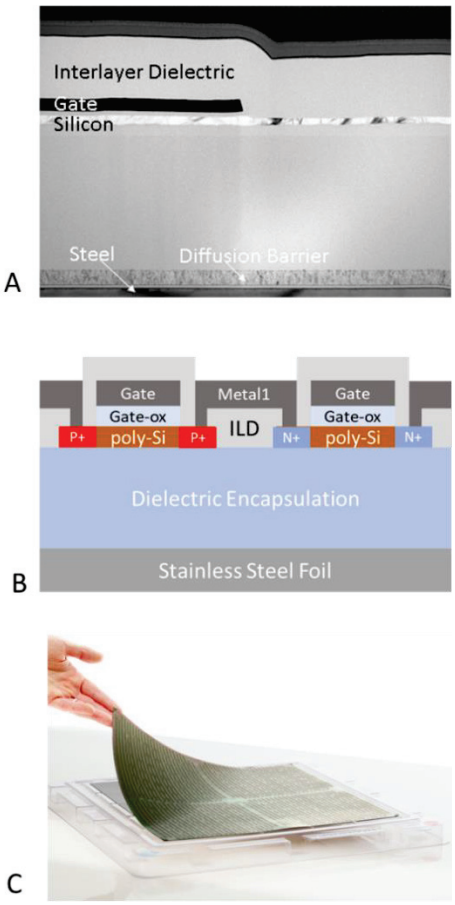

Fig. 1 SEM image showing the barrier layer on steel (A). Schematic of CMOS TFTs fabricated on steel (B), optical image of NFC devices fabricated on a flexible stainless steel sheet (C).

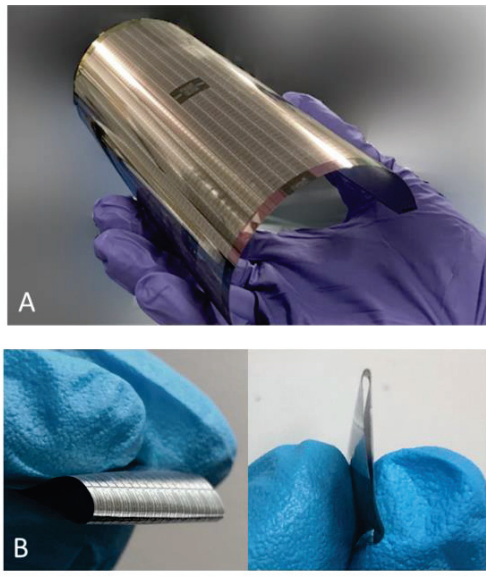

Fig. 2 Optical images of poly-Si CMOS devices on steel after thinning to 5 µm substrate thickness. 6x6" Sheet with the devices after thinning (A). Demonstrating bendability (B).

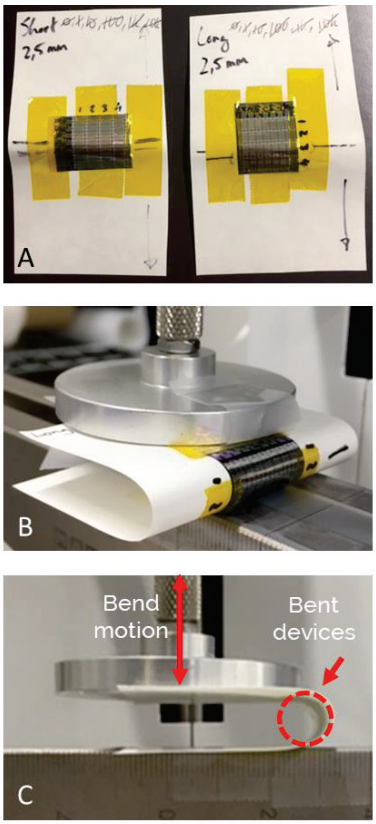

Fig. 3 Optical images of thinned samples taped on coupons for bend tests (A), bend test configuration from an angle (B), bend test configuration from the side showing bend radius (C).

We report on dynamic bend test results of individual NMOS and PMOS TFTs, where electrical parameters (threshold voltage (V_T), field effect mobility (μ_{FE}), subthreshold slope (S), and I_{on}/I_{min} ratio) are measured after various bend cycle sets. For these experiments, bends at 2.5R are chosen, and bending cycles of 1, 10, 100, 1,000 and 10,000 are investigated.

With a thickness of 5 µm, the strain on the top surface results in only 0.12% [8]. All measurements have been performed in flat condition. Tensile stress is studied in this paper, since ceramic materials such as silicon nitride and silicon oxide in general have a much larger compressive strain limit than the tensile strain limit. Two separate samples have been used to investigate the tensile strain in parallel to the channel (// -bend), and perpendicular to the channel (⊥ -bend). The worst-case scenario is explored where the devices on the sample are located on the very top of the substrate without an encapsulation layer that could reduce the device stress and shift the stress neutral plane toward the device layer. Bending tests are performed on a Mark-10 with custom fixtures to hold the experimental samples. Fig. 3 shows the bend-test configuration. Sample coupons were cut out from the larger sheet and taped onto a paper carrier for handling. The bend cycle frequency is approximately 0.15 Hz.

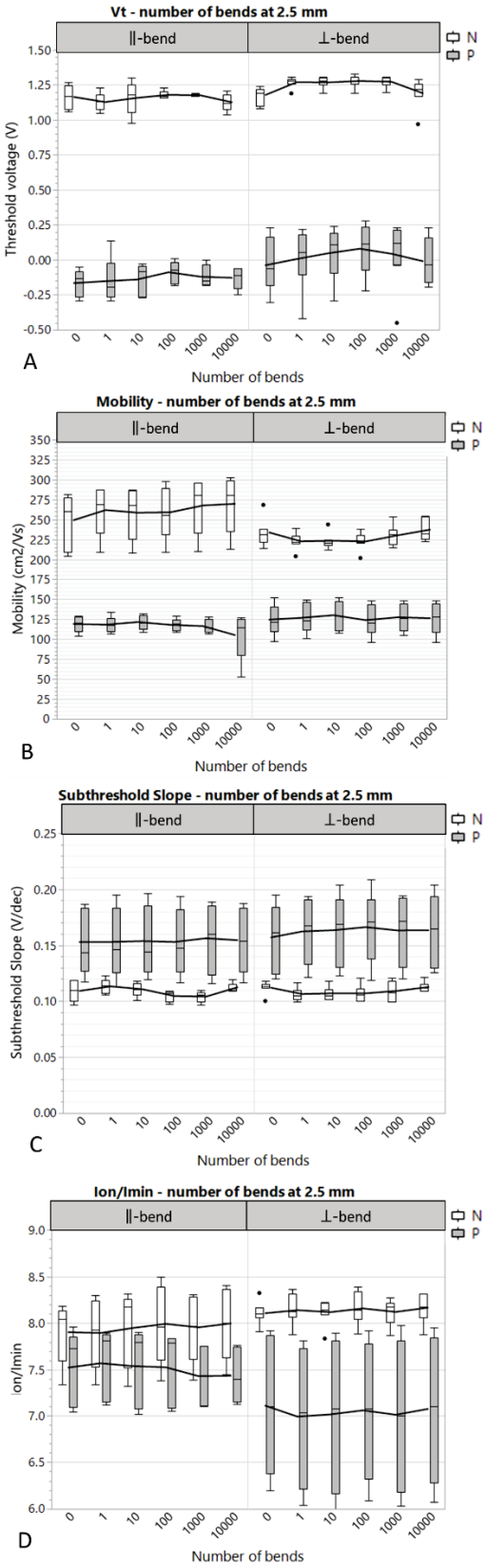

Fig. 4 NMOS and PMOS TFT bend cycle parameter extractions for both bend directions. Threshold voltage (A), field effect mobility (B), subthreshold slope (C), I_{on}/I_{min} ratio (D).

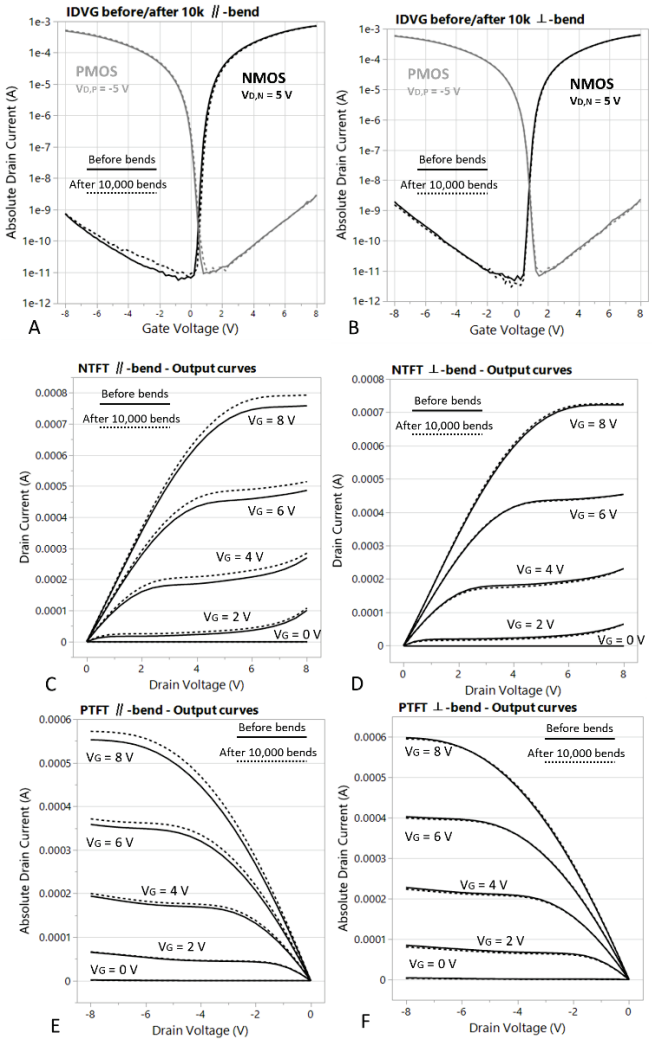

Fig. 5 NMOS and PMOS TFT transfer and output characteristics before bends and after 10,000 bends. TFT transfer // -bend (A), and ⊥-bend (B). TFT output. NMOS // (C) and ⊥(D)-bend, PMOS // (E) and ⊥(F)-bend.

3 RESULTS

Fig. 4 shows the box plots of the TFT parameters for both directions of the bend comparing each bend cycle set, including the values before bend. Both NMOS and PMOS TFTs are included in the graphs. Variation even after 10,000 bends is negligible and mainly caused by sample handling, which gives a high level of confidence in device reliability at such low bending radii. A representative device is taken from the sample set, and its transfer characteristics are plotted in Fig. 5a,b before and after 10,000 bends. The curves before and after the bend show no signs of degradation. Fig. 5c-f shows the output characteristics of NTFT and PTFT in both bend directions, again comparing the curves before bend, and after 10,000 bends. For this case, a slight increase in on-current is observed only for the // -bent sample. Although

the increase is limited, the cause of this increase has been researched in related works [5]. The on-current increase is attributed to an elongation of the lattice constant of silicon, which causes the energy bandgap to become smaller than it was before the stress was applied. The smaller bandgap energy relates to an increase in free carriers in silicon at a fixed temperature, and the activation energy of the channel is reduced. Other parameters that as a result would be impacted by this change are a mobility increase, and a threshold voltage decrease. According to our data however, for 10,000 bends at 2.5R this difference in the two other parameters cannot be clearly observed.

4 CONCLUSIONS

This work shows a first exploration towards increasing the flexibility of electronics manufactured on a stainless steel substrate. Dynamic tensile stress applied to the thinned samples at 2.5R for 10,000 bend cycles shows minimal impact to the TFT performance. Related works on polyimide with similar bend radii and cycle counts show higher device degradation [6]. Future work will involve lower bend radii and larger numbers of bend cycle investigations. The devices still have room for further flexibility improvement through a number of strategies, including the use of a passivation layer to improve the stress stability of the device layer.

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