A High Performance 3-bit Ripple Counter Circuit Based on Organic TFTs for Flexible Readout Integrated Circuit

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ABSTRACT

We propose a high performance 3-bit negative edge-triggered ripple counter based on Organic Thin Film Transistors (OTFTs). All the logic gate circuits used in this work are inverters and NAND circuits based on OTFTs with large zero-VGS load. A voltage range of 0 to 30V and a frequency of 12.5KHz clock signal is used for the ripple counter as input clock input. A high output level of ~27.4V and a low output level of ~4 or 5V are measured at the 2nd and 3rd stages' output node of the ripple counter. Their frequencies are one quarter and one eighth of the input signal's frequency. The output signal of the proposed ripple counter changes when its input signal falls to low level from high.

1 INTRODUCTION

Organic thin-film transistors (OTFTs) are of significant interest for applications in flexible electronics, especially in flexible displays, logic circuits for radio-frequency identification (RFID) tags, ADC in readout integrated circuit and smart sensors [1-6]. The key advantages of organic electronics, compared with silicon technology, are low-cost manufacturing, flexible substrates and large area production [7-8]. ADC is a fundamental component in integrated readout circuit. Ripple counter is a significant part of the ADC, just shown in Fig.1. In this work, we report the design, fabrication and characterization of a 3-bit negative edge-triggered ripple counter based on OTFTs, which is built by inverters and NAND circuits with large zero-VGS load. The proposed ripple counter shows good robustness and high performance.

2 ORGANIC TFT PROCESS AND PERFORMANCE

The device cross section of the top gate bottom contact (TGBC) OTFT is shown in Fig.2(a). The TFT fabrication process is as follows: A 50-nm-thick Au layer was first deposited on glass substrate by sputtering and then patterned using wet etching for source-drain electrodes, followed by spin-coated 60nm thick OSC and 300-nm-thick OGI. The 50-nm-thick Au was thermally-evaporated and then patterned for gate electrode. After that, a 100-nm-thick PVA followed by a 300-nm-thick SU8 photopolymer were spin-coated and patterned for passivation interlayer dielectric. After that, a 50-nm-thick Au was sputtered and patterned for the metal interconnect layer to created electrical connections where required between the metal layers. Finally, a third protective passivation layer was deposited. Fig.2(b) shows the optical image of the device with multiple source/drain fingers that can increase the conduction IDS without a large area overhead.

3 CIRCUITS DESIGN

All logic gates used to build the digital circuits described in this work are based on the zero-V_{GS} load inverter because of its low power consumption.

3.1 INVERTER AND NAND

The schematic and optical image of this inverter is presented in Fig.3(a). The OTFTs based inverter fabricated with W_D:W_L=800/2800 μm, where the load TFT is connected to have V_{GS}=0 V and is designed to be several times wider than the driver TFT. When the input voltage is high (i.e., GND), due to positive V_{th}, T_{Driver} is turned off, the output level is pulled to close to low (i.e., -VDD) because of the several times lager load TFT. When the input voltage is low, T_{Driver} provides a strong pull-up force and pulls the output level to high.

The design of NAND gates is built by adding a second driver transistor to the zero-V_{GS} inverter, its schematic and optical image are shown in Fig.3(b). The OTFT based NAND circuit fabricated with W_D:W_L=800:5600 μm. When the input level is high, the zero-V_{GS} connected T_{Load} pulls down the output node to low (i.e., GND). When input level is low, the T_{Driver} is turned on and pulls up the output node against the weak load offered by load TFT to VDD.

3.2 FLIP-FLOP

With the proposed OTFT based inverter and NAND circuits, we can further construct latches and flip-flops, which are important blocks in readout integrated circuits.

Fig.4(a) shows the schematic of the D Flip-Flop (DFF)

circuit using NAND and inverter together. The DFF circuit can be divided into two parts: (1) D latch and (2) SR latch, where D latch is master FF and SR latch is slave FF. Therefore, this FF can be called master-slave DFF. For D latch, when clock signal is pulled down to low, the output of the D latch equals to the input Data (D). For SR latch, the output changes when clock signal is pulled up to high. The operation of this DFF can be divided into two distinct periods; the pre-flip and flip periods. In the pre-flip period, as the clock signal goes down to low from high, NAND gates G1 and G2 in the master stage are turned on and G3 and G4 in the slave stage are turned off. The output of the master FF changes the output stage by receiving the input signal D. However, the slave FF is turned off and keep the original state. In the flip period, the clock signal is pulled high, NAND gates G1 and G2 in the master stage are turned off while NAND gates G3 and G4 in the slave stage are turned on. Therefore, the master FF is locked and the slave FF is turned on to receipt the output of the master FF. The output of DFF is synchronous flipped with the output of master FF due to slave FF being turned on. Therefore, the DFF we designed in this work is negative edge-triggered. Fig.4 (b) presents the optical image of the DFF.

3.3 3-BIT RIPPLE COUNTER

The 3-bit ripple counter can be easily implemented by connecting DFFs as shown in Fig.5. Each stage acts as a Divide-by-2 counter on the previous stage's signal. The Q node of each stage acts as both an output bit, and as an input clock signal for the next stage. Since the negative edge-triggered DFF is used to build the ripple counter, only when the clock signal falls to low level, the output of the ripple counter equal to D. In another word, the output signal changes after two periods at the input signal.

4 RESULTS AND DISCUSSION

Fig.6 shows the transfer characteristics of an OTFT with a channel width (W) and length (L) of 800 and 6 μm, respectively, the device exhibits a liner mobility (μlin) of 2.29 cm^2/Vs, threshold voltage (V_{th}) of 4.1V, and a high on/off current ratio 10_6. The μ_{lin} is extracted from the transconductance at V_{DS}=-0.1V. Fig.7 shows the measured output results of VDD of -5 and -10V of the OTFT based inverter. Fig.8 shows the measure dynamic characteristic of the OTFT based NAND circuit. In order to test the dynamic characteristic of the NAND circuit, we give two clk A and B of the same frequency with different delays to realize '00', '01', '10', '11' states. Only when A and B are both high, the output of the NAND circuit is low. In other cases, the output of the NAND is high. Fig. 9 shows the measured results of the 2nd and 3rd stages output of the ripple counter circuit at a clock frequency of 12.5 KHz. The output signal changes after two periods at the input signal.

5 CONCLUSIONS

In this work, we have developed a 3-bit negative edge-triggered ripple counter based on OTFTs. We have found that under a voltage range of 0 to 30 V and a frequency of 12.5 kHz clock signal, a high output level of ~27.4 V and a low output level of ~4 or 5 V are measured at the 2nd and 3rd stages' of the ripple counter. Their frequencies are one quarter and one eighth of the input signal's frequency. The output signal of the proposed ripple counter changes when its input signal falls to low level from high. With these three different frequency outputs, the ripple counter can count from 000 to 111. The proposed ripple counter can be readily implemented and is sufficiently robust for various applications.

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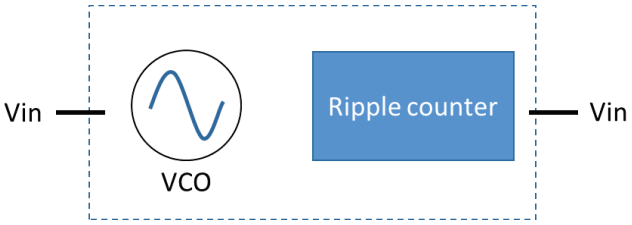

Fig. 1 Schematic of VCO based ADC

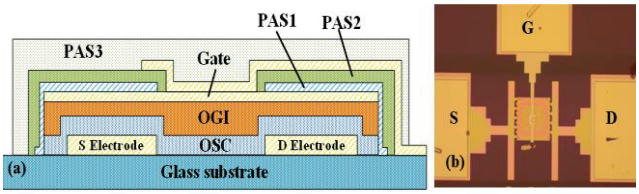

Fig. 2 Cross section and optical image of OTFT device

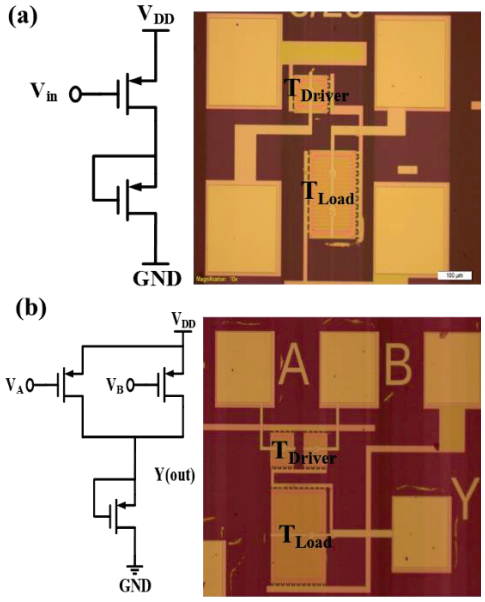

Fig. 3 Schematic and optical image of (a) inverter and (b) NAND circuits based on OTFTs

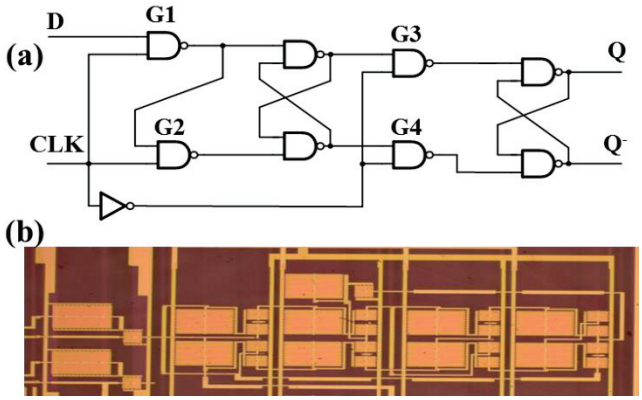

Fig. 4 (a) Schematic and (b) optical image of DFF

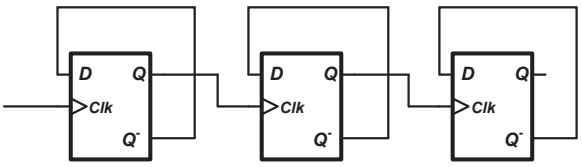

Fig. 5 Schematic of 3-bit ripple counter circuit

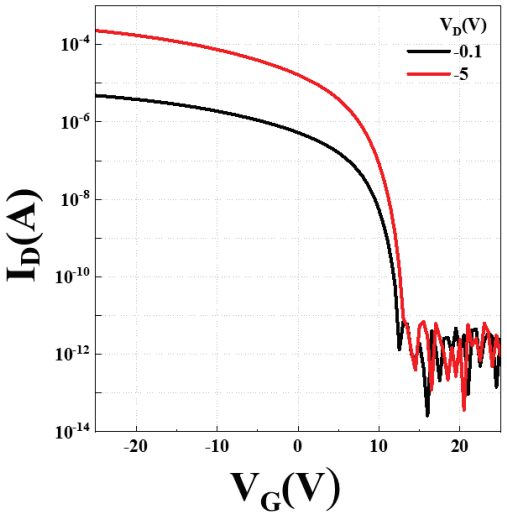

Fig.6 Transfer characteristic of OTFT

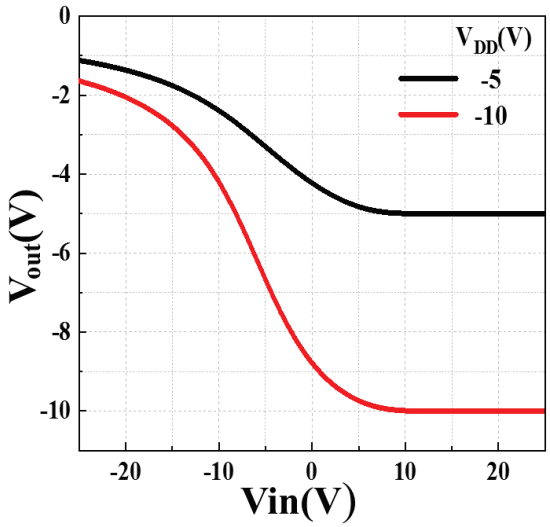

Fig.7 Output characteristic at VDD of -5 and -10V of the OTFT based inverter

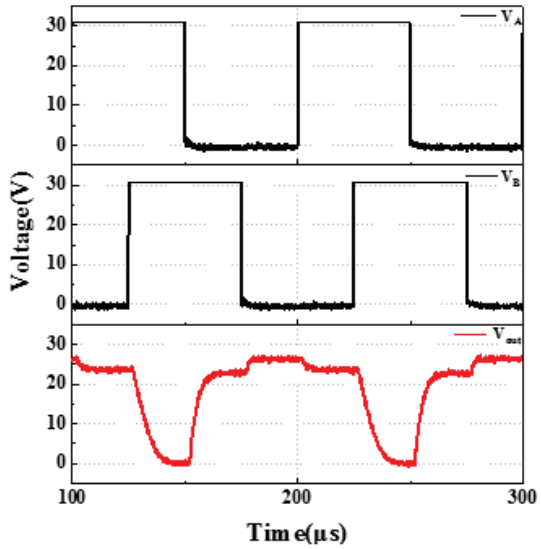

Fig.8 Measured dynamic characteristic of the OTFT based NAND circuit

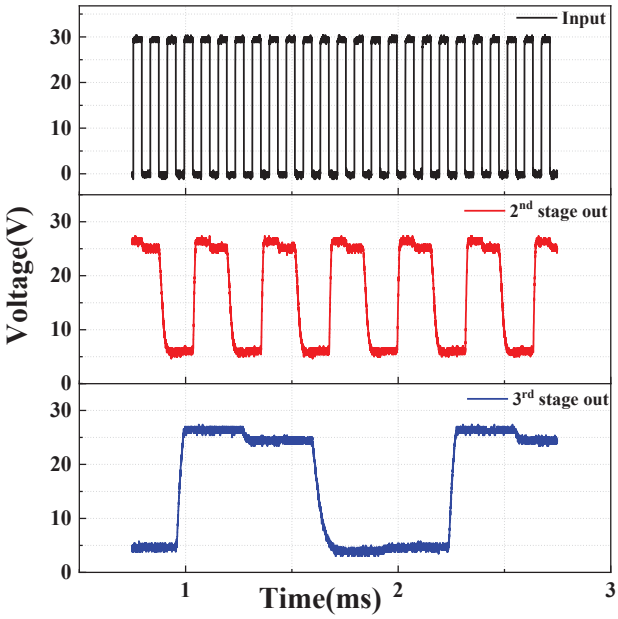

Fig.9 Measured results of 2nd and 3rd stage outputs of the ripple counter circuit