Effects of Annealing Gas on Electrical Properties of La_2O_3 Gate Dielectrics

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ABSTRACT

Solution-processed lanthanum oxide(La_2O_3) films were formed on the Si substrates under N_2 and O_2 ambience annealing conditions. Compared to N_2 conditions, flat-band voltage shifted to positive gate bias direction and leakage current was less for O_2 annealed devices resulted from the reduction of the oxygen-related trap sites in the film.

1 INTRODUCTION

Thin-film transistors (TFTs) with high-k dielectric have been studied for high mobility, low driving voltage, and large-sized display for next-generation display [1-3]. HfO_2, ZrO_2, Y_2O_3, Al_2O_3 and La_2O_3 have been considered as high-κ materials to replace SiO_2. Among them, La_2O_3 is excellent as the gate dielectric for high performance TFTs due to relatively high-κ value (~ 30) and large band gap (~ 6.0 eV) [4-5]. In addition, due to thermal stability with the silicon substrate it is difficult to form an interface with the silicon. However, There is a drawback of forming LaO (OH), $La(OH)_3$ by absorbing H_2O in the air. This disadvantage can be solved through oxygen treatment. [6] In the bond structure of La_2O_3 [7], it has oxygen vacancies (Vo). These oxygen deficiencies act as defects and adversely affect the electrical properties[8]. The device showed a decrease in electrical properties and a shift in the flat band voltage (V_{FB}) in the negative direction. In this study, La_2O_3 gate oxide was fabricated using a solution process that has the advantages of low cost and simple process. O_2 annealing process was performed to reduce Vo and annealing of inert gas N_2 was performed for comparison. In addition, by comparing the devices fabricated by the annealing time in a vacuum state, it was confirmed that the section in which the change in capacitance is the greatest, that is, the section to be densified. Accordingly, the electrical characteristics were analyzed by N_2 and O_2 annealing in order to confirm the influence of film densification and annealing ambient. Two kinds of metal-oxide-semiconductor (MOS-Cs) were compared and discussed.

2 EXPERIMENT

Al / La2O3 / p-Si MOS-C having the structure of Fig. 1 was fabricated and evaluated. P-type Si (100) substrate were cleaned via RCA(SC1,BOE,SC2) methods. The La_2O_3 solution was prepared by dissolving precursor of lanthanum nitrate hexahydrate ($LaN_3O_9H_2O$) in 2-methoxyethanol and stir at 1000 rpm for 5 hours at 80 ° C. Then, the prepared La_2O_3 solution was spin-coated at 3000 rpm for 30s. After pre-annealing for 10 min on a hot plate, post deposition annealing was performed with RTA for 20 minutes and 60 minutes at 400 ° C. under N_2 and O_2 ambient. The al electrode was deposited with a thickness of 70 nm and the width was deposited using a shadow mask having a dot size of 300 μm. Electrical properties of the films with annealing conditions were assessed by capacitance-voltage (C-V) measurements using an Agilent 4980A precision LCR meter and current density-voltage (J-V) measurements using an Agilent B1500A.

3 RESULT and DISCUSSION

Fig. 2 shows the 0, +, 2+ states of the 6-fold oxygen vacancy of La_2O_3.[7] La_2O_3 has two types of oxygen vacancy with 4 or 6 La neighbors. This vacancy creates an additional state that acts as a trap for electrons. Since these electron traps can also act as defects, the electrical properties will be improved if the oxygen vacancy can be treated. Fig. 3-(a) hysteresis of C-V characteristics of the samples fabricated using La_2O_3 oxide with N_2 and O_2 ambience annealing conditions. Through Table. 1 we confirmed that the oxide capacitance (C_{ox}) increased from 199.3 pF for N_2 conditions to 241.5 for O_2 annealing process. K value also increased from 22.2 to 27. After O_2 annealing, the V_{FB} shifted by 0.2 V in the positive direction compared to N_2 conditions. These results indicate that the O_2 annealing effectively reduces the positively charged Vo in the La_2O_3 films. Also, the hysteresis width was smaller than the N_2 ambient. The V_{FB} shifted in the positive direction by 0.8V in the O_2 ambient and 1.2V in the N_2 ambient, and the electron trap was reduced by shifting the O_2 ambient by 0.4V less than the N_2 ambient. These results suggest that annealing in the O_2 ambient effectively reduced oxygen vacancy.

Fig 3-(b) shows C-V indicating whether oxygen treatment has an effect on time. We annealed at 10minute intervals for 10~60 minutes and confirmed that the films were most densified between 20 and 60 minutes and the electrical properties were confirmed by annealing in two ambient. Table 1 shows that V_{FB} has almost the same value depending on the annealing

ambient. This result indicates that oxygen treatment takes place independently of the large densification of the film. Fig 4 shows the J-V curve of the device. Leakage current was checked at -1 V and 3.69×10^{-7} at 20 min in O_2 annealing process, 2.26×10^{-7} at 60 min 4.91×10^{-6} at 20 min 6.60×10^{-7} at 60 min each in comparison, both cases decreased in oxygen ambient. These result show that gate oxide is stabilized by reducing the Vo which are electron conducting path through the dielectric. Fig.5 shows interface trap density (D_{it}) of the samples performed to confirm the interfacial properties between La_2O_3 and Si substrate. D_{it} is extracted by Terman method and is represented by the following equation:

$$D_{it} = \frac{C_{ox}}{q^2}\left(\frac{dV_G}{d\phi_s} - 1\right) - \frac{C_S}{q^2} = \frac{C_{ox}}{q^2}\frac{d\Delta V_G}{d\phi_s}, C_s = \frac{C_{ox}C_{hf}}{C_{ox}-C_{hf}}$$ [9].

We found that the O_2 annealing process played a role of reduction of the D_{it} values from 9.83×10^{11}cm^2 / eV^{-1} to 7.65 × 10^{11} cm^2/eV^{-1}. These results imply that the Vo at the interface were treated during the annealing in the O_2 conditions.

4 CONCLUSIONS

We investigated the effect of annealing gas conditions and time on the electrical properties of La_2O_3 gate dielectrics. The Cox values were higher and the leakage current was lower for O_2 annealed devices than that of N_2 annealed samples. These results show that O_2 annealing process reduces Vo in the La_2O_3 films resulting in excellent electrical properties of the devices. Based on the experimental results, we strongly recommend La_2O_3 films formed with O_2 annealing process as a gate insulator for TFT applications.

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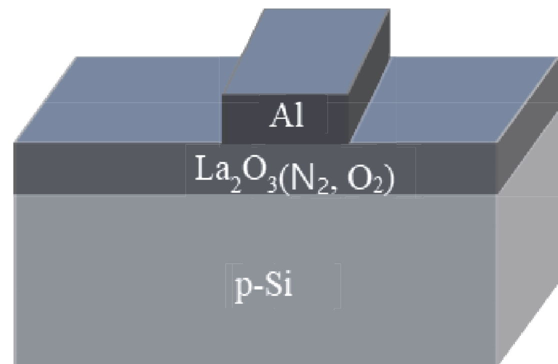


Fig. 1. Structure of metal-oxide semiconductor

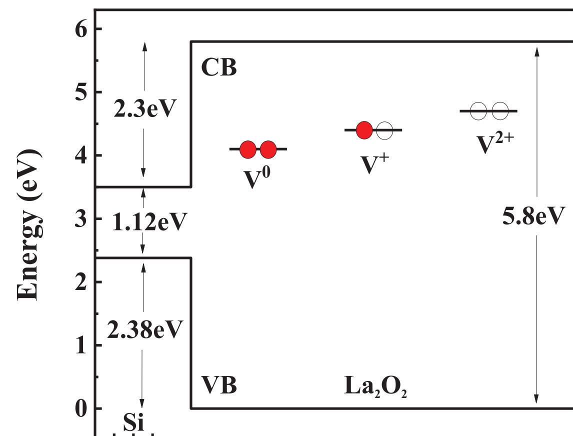
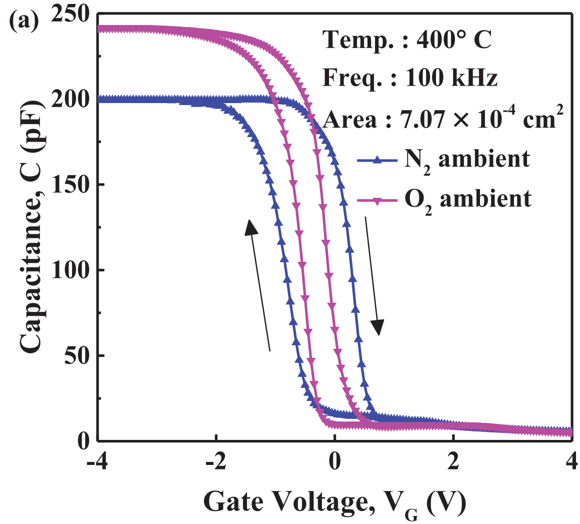


Fig. 2. Energy levels of 6-fold coordinated oxygen vacancy in La_2O_3



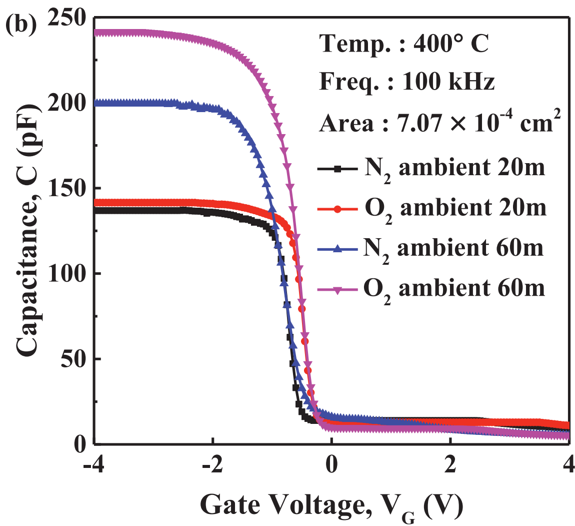


Fig. 3. C-V characteristics (a) Hysteresis of annealing for 60 minutes in N_2, O_2 ambient (b) 20 minutes 60 minutes annealing in N_2, O_2 ambient

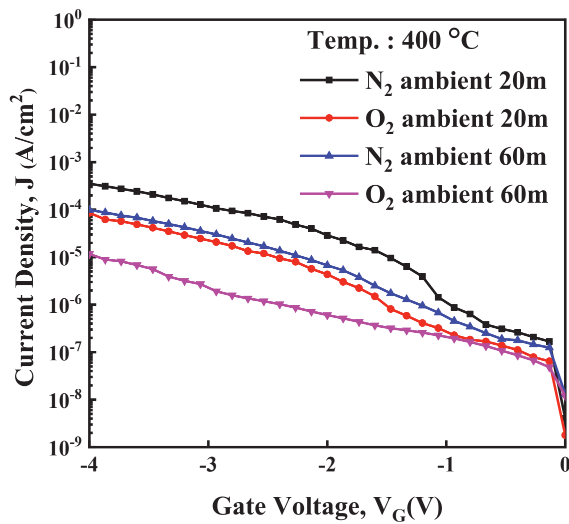


Fig. 4. J-V characteristics of La_2O_3 films annealed for 20 minutes and 60 minutes in N_2 and O_2 ambient

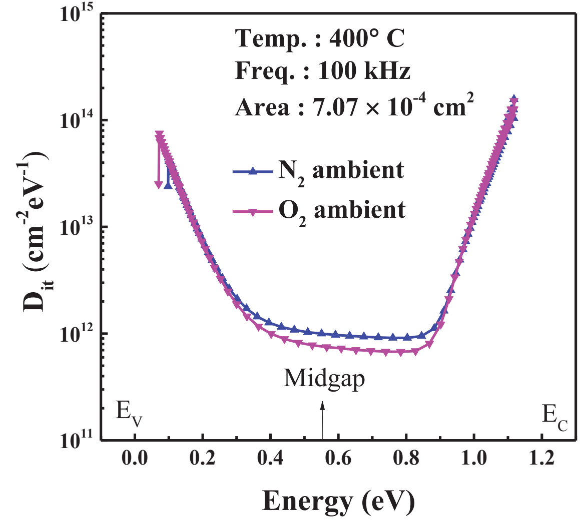


Fig. 5. D_{it} characteristics of N_2 and O_2 annealed La_2O_3 films

Table. 1. Extract of electrical parameters by annealing time and ambient

	N_2 20m	O_2 20m	N_2 60m	O_2 60m
Capacitance (pF)	136.8	141.4	199.3	241.5
κ	21.8	22.1	22.2	27.0
EOT (nm)	17.8	17.2	12.2	10.1
V_{FB}(V)	-0.62	-0.48	-0.66	-0.38
D_{it} (cm^{-2}eV^{-1})	-	-	9.83 $\times 10^{11}$	7.65 $\times 10^{11}$
Leakage current (A/cm^2)	4.91 $\times 10^{-6}$	3.69 $\times 10^{-7}$	6.78 $\times 10^{-7}$	2.26 $\times 10^{-7}$