A study on gray level dependence of influence due to flexoelectric effect in FFS LCDs

Daisuke Inoue, Tomomi Miyake, Mitsuhiro Sugimoto

Tianma Japan, Ltd., 1-1-2, Kashimada, Saiwai-ku, Kawasaki, Kanagawa, 212-0058, Japan

Keywords: FFS mode, Flexoelectric effect, Gray level dependence, Image-sticking, Flicker shift

ABSTRACT

Though transmittance dependency of DC offset voltage that relate to image sticking made a quadratic function, its bottom position and flicker minimum DC offset voltage depend on gray level due to flexoelectric effect. We demonstrated influence of flexoelectric effect changes depending on slit electrode width and black matrix width.

1 INTRODUCTION

Good image quality is provided by both in-plane switching (IPS) mode liquid crystal displays (LCDs) [1] and fringe-field switching (FFS) mode LCDs [2], which are derived from IPS mode LCDs. However, FFS mode LCDs are superior to IPS mode LCDs in terms of driving voltage and response time. The former is lower and the latter is faster for FFS mode LCDs because of their strong electric field near the substrate with slit electrodes. For this reason, FFS mode LCDs have been widely used for various applications, such as mobile phones, tablets, monitors, televisions and in-vehicle displays. However, the FFS mode is more susceptible to the image-sticking problem than other LCD modes. Furthermore, there is the flicker shift problem peculiar to FFS mode LCDs.

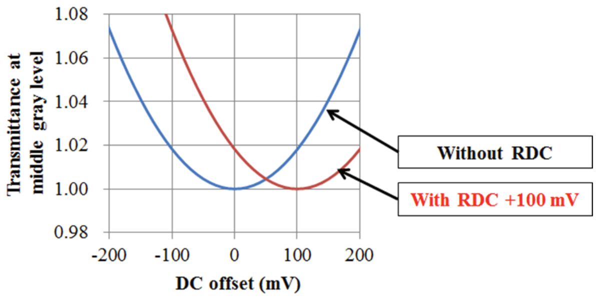

Fig. 1 Transmittance dependency of DC offset voltage.

Although several causes of image-sticking in LCDs are well known, we believe the most important cause is residual DC (RDC) voltage. When RDC is generated, positive and negative voltages applied to a liquid crystal (LC) layer become asymmetric. Similarly, these voltages become asymmetric when external DC voltage is applied. As shown in Fig. 1, transmittance at low or middle gray level changes like a quadratic function when DC offset voltage is applied. Hereafter, we call this DC offset-transmittance property varying like a quadratic function, D-T property. Image-sticking can be estimated by displaying various gray levels after displaying a checker flag pattern for a specified time in general. However, if amounts of RDC become different between adjacent black and white patterns, the boundary between them becomes visible. This is the image-sticking problem caused by RDC [3].

Flicker shift is a phenomenon in which common electrode voltage (hereafter, the "Vcom") of flicker minimum changes with time and saturates after adjusting Vcom to minimize the flicker value.

These image-sticking and flicker shift relate to flexoelectric effect in which LC director direction changes between positive and negative frames due to electric field and polarization generated by distortion such as splay deformation or bend deformation [4]. We demonstrated that flexoelectric effect affects to image-sticking caused by RDC because the bottom positon of D-T property changes depending on gray level when transmittance difference between positive and negative frames occurs due to flexoelectric effect [5]. Similarly, flicker minimum DC offset voltage changes depending on gray levels when transmittance difference occurs [6].

In this paper, we discuss gray level dependency of D-T property and flicker minimum DC offset voltage thorough computer simulation changing cell parameters such as slit electrode width and black matrix (BM) width in FFS mode LCDs. Furthermore, we measured D-T property and flicker minimum DC offset voltage of LCD panel and compared with simulation results.

2 EXPERIMENT and SIMULATION

2.1 Method of measuring D-T property and flicker minimum DC offset voltage at each gray level

We measured D-T properties and flicker minimum DC offset voltages at 32 Gray, 64 Gray and 128 Gray. The LCD panel was driven by static driving, which applies DC +20 V to the gate line. The gate was always open and driven by square waves produced by a function generator. Static driving is AC driving method that is free from influence of feed through voltages because the gate voltage is constant during measurement.

It is possibility to generate RDC voltage between pixel and common electrodes during measurement of D-T property and flicker minimum DC offset voltage, because DC voltage is applied while short time. We always keep applying AC 0.01 V without DC voltage between pixel and common electrodes before we measure one point of data such as transmittance and flicker. Then, check the flicker minimum DC offset voltage at 128 Gray level before and after the measurement and confirm that RDC is not generated.

2.2 Simulation method of D-T property and flicker minimum DC offset voltage

We simulated the D-T property and flicker minimum DC offset voltage in the FFS cell depicted in Fig. 2 using cell and LC parameters shown respectively in Table 1 and Table 2. We carried out these simulations with the simulation software LCD-Master 2D by Shintech, Inc.

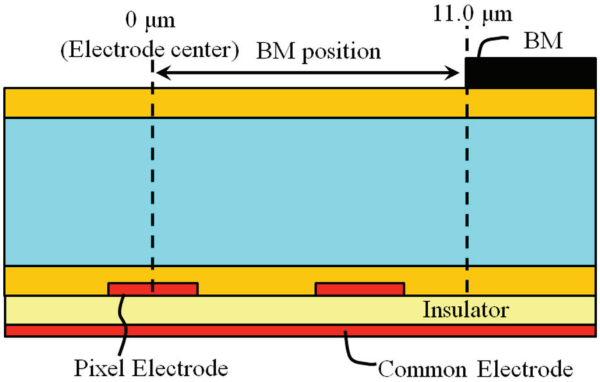

Fig. 2 Simulation model of FFS cell.

The flexoelectric effect was added LCD-Master 2D in the next formula, and we used the flexoelectric coefficient of es and eb as +10 pC/m, respectively.

$$\boldsymbol{P}_f = e_s \cdot \boldsymbol{n}(\nabla \cdot \boldsymbol{n}) + e_b \cdot \boldsymbol{n} \times (\nabla \times \boldsymbol{n})$$

$\boldsymbol{P}_f$: Flexoelectric polarization

e_s and e_b : Splay and bend flexoelectric LC coefficients

$\mathbf{n}$: Vector description of the LC director

Table 1 Cell parameter of FFS cell

Insulator	Thickness	300 nm	
	ε	6.0	
Pixel electrode	Pitch	7.0 μm	
	Width	2.6 μm	3.0 μm
	Space	4.4 μm	4.0 μm
Alignment layer	Thickness	100 nm	
	ε	3.3	
BM position (width)		0 – 11μm	
Slit angle (LC director)		7 deg.	

Table 2 LC parameter

ε parallel	7.4
ε perpendicular	2.8
K11	14.2 pN
K22	7.1 pN
K33	16.0 pN
γ1	61 mPa･s
es	+10 pC/m
eb	+10 pC/m

We first simulated the Voltage-Transmittance (V-T) property to calculate each of the gray level voltages using static analysis mode of LCD-Master 2 D. We averaged V-T properties of plus and minus voltage because they are not equal due to flexoelectric effect. Then we defined gray level 0 as black and gray level 255 as white and calculated each gray level to have gamma value of 2.2. The calculated results at gray level are shown in Table 3.

Table 3 Simulation results of gray level voltage

Gray level	AC voltage
32 Gray	1.6 [V]
64 Gray	2.0 [V]
128 Gray	2.6 [V]
255 Gray (White)	5.3 [V]
VT peak voltage	5.7 [V]

We then executed D-T property and flicker minimum DC offset voltage using dynamic analysis mode of LCD-Master 2 D. Although we suppose refresh rate 60 Hz as driving frequency, we set one period of a driving frame at 16.6 ms for convenience sake. In case of D-T property simulation, we first calculated transmittance at each gray level with DC offset voltage of three points (-100 mV, 0 mV, +100 mV, respectively) by averaging the transmittance of each of the positive and negative frames after the transmittance waveform stabilized. And then we calculated bottom position of D-T property by fitting transmittance of three points with a quadratic function.

We find flicker minimum DC offset voltage at each gray level to repeat simulation changing DC offset voltage until we obtain flicker minimum transmittance waveform. Resulting D-T property and flicker minimum waveform are shown in Fig. 3 and Fig. 4, respectively.

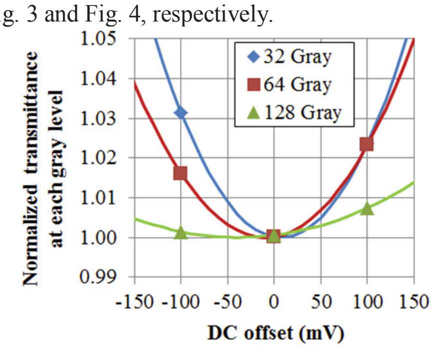

Fig. 3 D-T property simulation results at each gray level

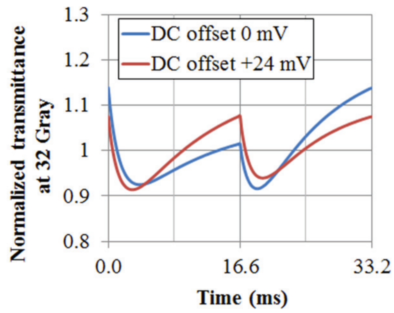

Fig. 4 Flicker minimum waveform simulation results

3 RESULTS and DISCUSSION

3.1 D-T property and flicker minimum DC offset voltage measurement results

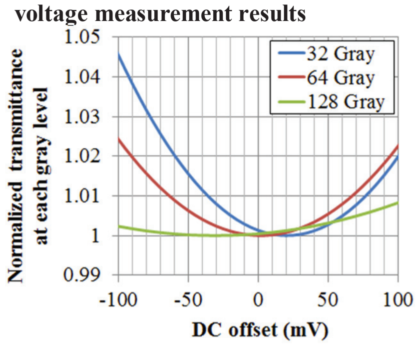

Fig. 5 Measurement results of D-T property

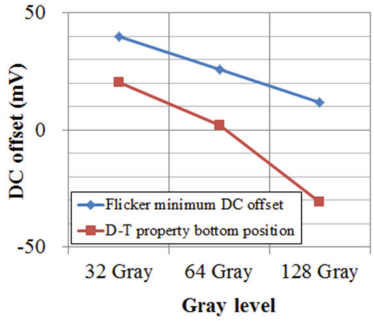

Fig. 6 Measurement results of flicker minimum DC offset voltage and D-T property bottom position

Measurement results of D-T property for each gray level are shown in Fig. 5, and measurement results of flicker minimum DC offset voltage and D-T property bottom position are shown in Fig. 6. D-T property and flicker minimum varied depending on gray levels. We also find that they are positioned on the plus side at 32 Gray and change to the minus direction at 128 Gray. We executed simulation varying slit electrode width to investigate the cause of gray level dependency.

3.2 D-T property and flicker minimum DC offset voltage simulation results

Simulation results of D-T property bottom position and flicker minimum DC offset are shown in Fig. 7 and Fig. 8, respectively. BM position is 11 μm, which is matched to our LCD using the measurement, in this simulation. Both of them show gray level dependency due to slit electrode width w and the dependency is larger at w=2.6 μm than at w=3.0 μm.

Fortunately, gray level dependencies of simulation results at electrode width w=2.6 μm are similar to their of measurement results in both of D-T property bottom position and flicker minimum DC offset voltage. We believe that electrode width of LCD using measurement is nearly 2.6 μm.

We simulated D-T property bottom position and flicker minimum DC offset voltage varying BM width to understand the gray level dependency of them. As shown in Fig. 9 and Fig. 10, D-T property bottom positions of each gray level fluctuate at 7 μm period of BM position, which is coincident with electrode pitch. We also found that bottom positions at each gray level almost correspond at w=3.0 μm, but do not correspond at w=2.6 μm.

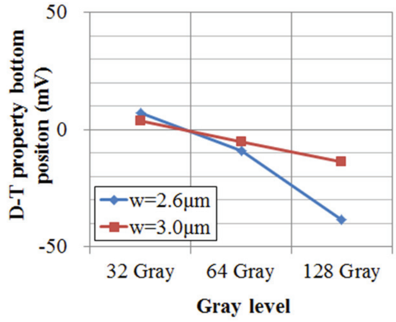

Fig. 7 Simulation results of D-T property bottom position for different electrode width

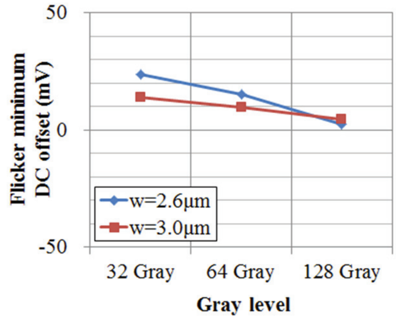

Fig. 8 Simulation results of flicker minimum DC offset voltage for different electrode width

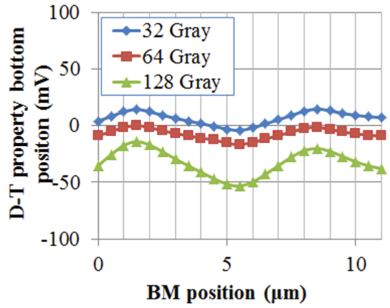

Fig. 9 Simulation results of D-T property bottom position varying BM position for each gray level (w=2.6 μm)

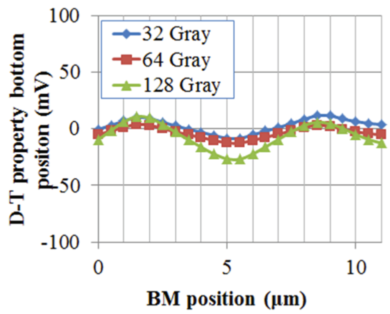

Fig. 10 Simulation results of D-T property bottom position varying BM position for each gray level (w=3.0 μm)

Simulation results of flicker minimum DC offset with electrode width w=2.6 μm are shown in Fig. 11. Flicker minimum of each gray level also fluctuate at 7 μm period of BM position like the result of D-T property bottom position, but difference at each gray level is smaller than that of D-T property bottom position.

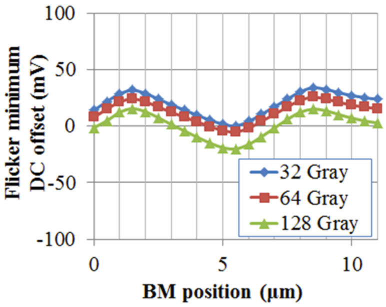

Fig. 11 Simulation results of flicker minimum DC offset varying BM position for each gray level (w=2.6 μm)

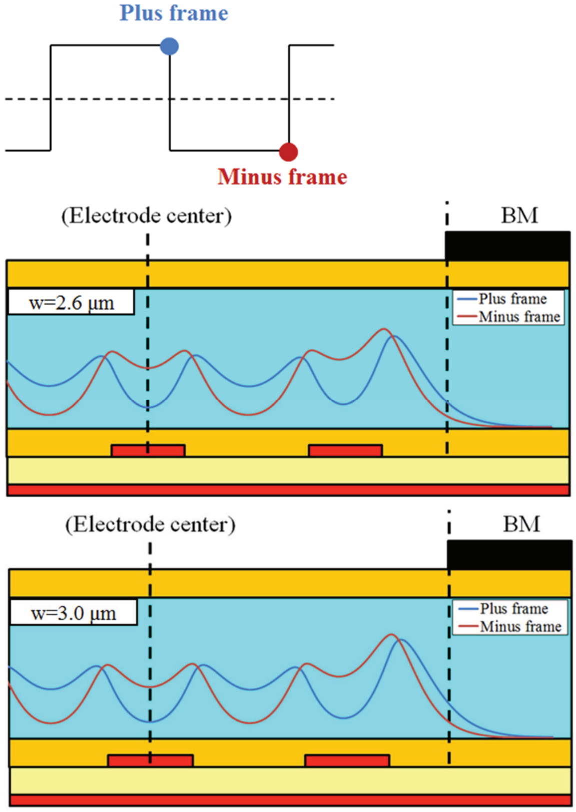

Fig. 12 Simulation results of pixel profile at plus frame and minus frame for different electrode width at 128 Gray.

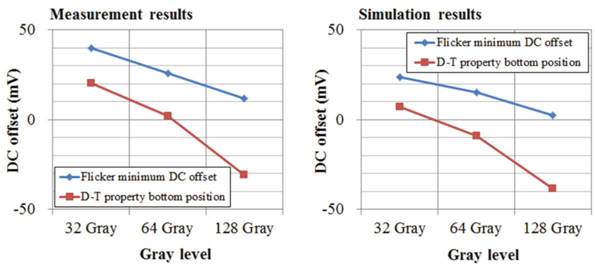

Fig. 13 Measurement and simulation results comparison of D-T property bottom position and flicker minimum

Transmittance profile simulation results at 128 Gray are shown in Fig. 12. Transmittance of plus frame at pixel electrode center and minus frame at slit center fall and that of opposite frame at each position rise due to flexoelectric effect. In case of w=3.0 μm (lower drawing), transmittance profile of plus (or minus) frame at electrode center is similar to that of minus (or plus) frame at slit center, but in case of w=2.6 μm (upper drawing), both are not the same. We believe that D-T property bottom position and flicker minimum DC offset of gray level dependence can suppress due to optimization of electrode width to cancel out the transmittance change between plus and minus frames caused by flexoelectric effect.

At the last, we compare the measurement results and simulation results of D-T property bottom position and flicker minimum DC offset voltages. As shown in Fig. 13, although tendencies against gray levels of these results are similar, we can confirm the difference, e.g. flicker minimum DC offset at 128 Gray is +10 mV in the measurement result, but that is about 0 mV in the simulation result.

We believe that there is some charge up in some layer or on some interface between pixel and common electrode from the difference. There is a possibility that this charge up affects to flicker shift in FFS mode

4. CONCLUSION

In this paper, we discussed the gray level dependency of D-T property and flicker minimum DC offset voltage. We demonstrated to cancel the transmittance difference of plus and minus frames due to flexoelectric effect to optimize the electrode width.

Although we measured and simulated about D-T property and flicker minimum DC offset voltage, through comparison measurement results with simulation results at the same time, we verified that it is possible to separate the influence of flexoelectric effect and the other factors.

REFERENCES

[1] M. Oh-e and K. Kondo, “Electro-optical characteristics and switching behavior of the in-plane switching mode,” Appl. Phys. Lett., **67**, pp. 3895-3897 (1995).

[2] S. H. Lee, S. L. Lee and H. Y. Kim, “Electro-optic characteristics and switching principle of a nematic liquid crystal cell controlled by fringe-field switching,” Appl. Phys. Lett., Vol. 73, pp. 2881-2883 (1998)

[3] Shin, Y., Jung, M., Jeon, B., Shin, K., and Roh, N., “ An Analysis Method of Image Sticking of LCD,” In SID Symposium Digest of Technical Papers, Vol. 47, No. 1, pp. 1693-1696 (2016)

[4] K. T. Huang, Y. W. Huang, R. X. Fang, Y. T. Chao, T. Lee, C. Lee and T. S. Jen, “Investigation on the Flexoelectric Effect of LC in the Localized Area of FFS Pixel Structure,” In SID Symposium Digest of Technical Papers, Vol. 46, No. 1, pp. 1559-1562 (2015)

[5] R. B. Meyer, “Piezoelectric effect in liquid crystals”, Phys. Rev. Lett. 22(18), pp. 918-921 (1969)

[6] D. Inoue, T. Miyake and M. Sugimoto, “Novel viewpoints on image sticking caused by residual DC voltage in FFS mode LCDs”, Proceedings of the International Display Workshops, Vol. 25, pp. 140-143, (2018)