Oral Presentation

[AMD4]Emerging TFTs

Chair: Hyun Jae Kim (Yonsei Univ.)
Co-Chair: Yosei Shibata (Tohoku Univ.)
Thu. Nov 28, 2019 9:00 AM - 10:20 AM Mid-sized Hall B (1F)

9:50 AM - 10:05 AM

[AMD4-4L]Integrated Polycrystalline Silicon Photomask Technology for Low-Temperature Polycrystalline Silicon (LTPS) TFTs

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Keywords:LTPS TFTs, Hybrid Backplane, LTPO

A novel Four-Photomask complementary metal oxide semiconductor (CMOS) technology for low temperature polycrystalline silicon (poly-Si) thin film transistors (LTPS TFTs) was proposed in the first time. The combination of poly-Si layer and P plus (P+) region definitions within one lithography process was realized by a half-tone photomask. In this paper, the characteristics of TFTs within a half-tone Poly-Si Photomask of lithography processes were reported and compared with electrical characteristics of typical Six-Photomask lithography processes. The Integrated Poly-Si Photomask Technology can be applied to reduce the numbers of photomask of making an IGZO and LTPS Hybrid TFTs Array.