Poster Presentation

[AMDp1]Oxide TFTs

Thu. Nov 28, 2019 10:40 AM - 1:10 PM Main Hall (1F)

10:40 AM - 1:10 PM

[AMDp1-10]Analysis and Solution of 4/5/6 levels related issues in a-IGZO TFT Gate Driving Circuits for 32-in FHD TFT-LCD

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In this paper, 4/5/6 levels related issues in two different a-IGZO TFT gate driving circuits for 32-in FHD TFT-LCD have been analytical and settled. The two different circuits are called GOA_A (STT structure) and GOA_B (big channel length structure), respectively. Both GOA_A and GOA_B circuits have the phase problem at 4/5/6 levels in TD1, and these phase problems have been settled in TD 2 by regulating the HVA signal voltage. The horizontal line at 4/5/6 levels can only be found in GOA_B of TD1 and these horizontal line at 4/5/6 levels have also been solved in TD 2, while GOA_A have no such problems in TD1 and TD2. The details can be presented in this paper.

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