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Poster Presentation

## [AMDp2]Active-Matrix Devices

Thu. Nov 28, 2019 2:30 PM - 5:00 PM Main Hall (1F)

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### [AMDp2-11]Analysis of Horizontal-Mura Caused by Reset' s Abnormal Delay of GOA Output

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Keywords:Gate Driver on Array, Horizontal-Mura, Leakage Current, Array Design

A rare failure named Horizontal-Mura Caused by Reset' s abnormal Delay of GOA Output is studied systemically. By increasing frame frequency, changing TFT size ratio and increasing channel Length, the leakage current of voltage Gout' s Gate (PU) can be reduced, and Mura phenomenon can be significantly alleviated.