Poster Presentation

[AMDp2]Active-Matrix Devices
Thu. Nov 28, 2019 2:30 PM - 5:00 PM Main Hall (1F)

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[AMDp2-13]A Narrow Border Design and Low Power Consumption of a-Si:H TFT Gate Driver Circuit

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In this paper, an integrated hydrogenated amorphous silicon (a-Si:H) thin-film transistor (TFT) gate driver circuit design for narrow border and low power consumption in the small-size panel is proposed. The border can be decreased from 1 mm to 0.8 mm, which can be further improved to 0.65 mm. In addition, the power consumption of circuit can be reduced by using the 25% duty ratio 8 clock signals with high reliability.

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