Current Status on the n/p Type Oxide Semiconductor Materials and the Associated Devices Using Atomic Layer Deposition

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ABSTRACT

Atomic Layer Deposition (ALD) has been introduced for oxide semiconductor synthesis and the device applications. Interestingly, ALD enable to deposit not only high-performance oxide semiconductor (a-IGZO etc.) but also p-type oxide semiconductors (CuO and SnO) at low deposition temperature. It will have a great potential to solve the current material and device issues. ALD will be the emerging thin film process in the coming display application.

1 INTRODUCTION

On these days, display industries have rapidly adopted high performance amorphous oxide semiconductors (AOS, such as amorphous InGaZnO semiconductor) as an active layer in AMOLED, AMLCD, and flexible active matrix device applications [1-2]. Among various thin film deposition methods, Atomic Layer Deposition (ALD) has remarkably developed in semiconductor and nano-structure applications since early 1990 [3-4]. The unique properties, including controlling atomic-level-thickness, manipulating atomic-level-composition control, and depositing impurity-free films uniformly, may accelerate ALD related industries and applications in functional thin film markets. One of big and challenging markets, display industry, has been just started to look at the potential to adopt ALD based films in emerging display applications, such as transparent and flexible displays.

In this work, it will present the recent progress of OS materials and the associated device application. Unlike commercial sputtering method, atomic layer deposition (ALD) can make an opportunity to enhance not only device performances but also flexible properties. Firstly, it will show various oxide semiconductors deposited by ALD and compare with their semiconductor properties and device performances. Also, several multicomponent oxide semiconductors (such as ZnSnO, InZnO, InGaO, InZnSnO, InGaZnO etc.) [3], deposited by super cycle ALD methods, will be discussed regarding process issues vs. material properties. The flexible oxide semiconductor thin film transistors will be presented via ALD methods and the device may be evaluated by mechanical stresses such as bending radius and mechanical fatigue. Secondly, it will introduce atomic layer deposited p-type oxide semiconductors (CuO and SnO)[5-6] and the associated device performances. This work will be an important suggestion for novel thin film process such as ALD for the emerging display applications.

2 EXPERIMENT

The IGZO thin films were deposited by PEALD [7] using (3-dimethylamimopropryl)-dimethyl indium (DADI) as the indium precursor, diethylzinc (DEZ) as the zinc precursor, trimethylgallium (TMGa) as the gallium precursor, and O2 plasma as the reactant on a Si(100) substrate with a native oxide layer after acetone washing. The number of InOx subcycles were varied from 4 to 20, and the ZnO and GaOx were deposited one cycle immediately following each InOx cycle. The supercycle which consists of InOx, ZnO, GaOx subcycle [metal precursor pulse − Ar purge − O2 plasma − Ar purge] is processed as [InOx × n cycle − ZnO × 1 cycle − GaOx × 1 cycle], where n increased from 4 to 20 with a step of 4. The deposited samples are represented as IGZO0.3nm to IGZO1.8nm according to the thickness of the In2O3 sublayer calculated by GPC. Spectroscopic ellipsometry (SE) (Elli-SE(UV)-FM8) was conducted to analyze the thickness of the thin films. The microstructure of the IGZO thin films were investigated using transmission electron microscopy (TEM) (JEM-2010F, JEOL). The 20 nm IGZO active layers from IGZO0.3nm to IGZO1.8nm were grown at 200 °C and patterned using a combination of wet-etching and photolithography processes. Sputter-deposited indium tin oxide (ITO, 100 nm) source and drain electrodes were patterned by a lift-off method. The channel width (W) and length (L) dimensions were 40 and 20 μm, respectively. The electrical properties of the devices were measured using a HP 4155A parameter analyzer at room temperature. Flexible bottom-gate top-contact IGZO1.8nm TFTs were produced on a polyimide (PI) substrate. The thickness of the ITO gate layer was 100 nm, which was deposited by sputtering. The 100 nm Al2O3 dielectric layer was grown by thermal ALD at 200 °C using trimethylaluminum and H2O. All layers including gate, insulator, semiconductor, and source-drain layers were patterned by photolithography and wet-etching process.

3 RESULTS

A schematic of the stacked IGZO structure fabricated with layer-by-layer PEALD is shown in Figure 1b. Here, the concept of supercycle is used to represent [InOx × n cycle − ZnO × 1 cycle − GaOx × 1 cycle]. Since the growth rate per cycle (GPC) of each oxide layer is different (0.08 nm/cycle for InOx subcycle, 0.12 nm/cycle for GaOx subcycle, and 0.22 nm/cycle for ZnO subcycle), the GPC of the supercycle (Figure 1c) increased from 0.61 to 1.73 nm/ cycle as the number of In2O3 subcycles was increased from 4 to 20. It should be mentioned that the GPC of the supercycle measured experimentally perfectly fits the GPC of the supercycle calculated through the proportioned sum of the GPC of each subcycle. Such a result has not been commonly reported in previous thermal ALD-grown multicomponent oxide materials, in which the experimentally obtained GPC of the supercycle is usually dramatically less than the calculated GPC.

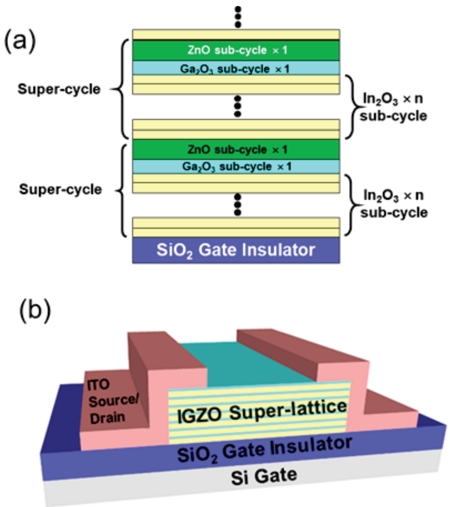

Figure 1. (a) schematic of PEALD IGZO stacked structure using the concept of super-cycle [InO_x × n cycle– ZnO × 1 cycle – GaO_x × 1 cycle] (b) schematics of ALD IGZO TFT structure.

Compared to polycrystalline In2O3 thin films with a cubic structure, IGZO thin films with embedded Ga–Zn–O layer (shown in Figure 2a) exhibit distinct disorder. The transmission electron microscope (TEM) images of the IGZO1.8nm thin film (Figure 2b,c) exhibit amorphous nature. Such a c-axis growth is reasonable since ALD's layer-by-layer deposition system can naturally promote c-axis growth with alternating layers of indium oxide and gallium zinc oxide. In addition, the IGZO1.8nm film exhibits uniform and homogeneous distributions of the chemical components, implying In diffusion through the ultrathin Ga −Zn−O layer, which further suppresses crystal growth. Additionally, sparse-density or void (pore) regions, which are commonly reported in sputtered IGZO thin film28 (probably due to plasma damage), were not observed in the cross-sectional image of the PEALD-grown IGZO thin films. The absence of such a less dense texture is attributed to the inherent characteristics of the ALD method that make it possible to deposit high-quality thin films with high density and few defects.

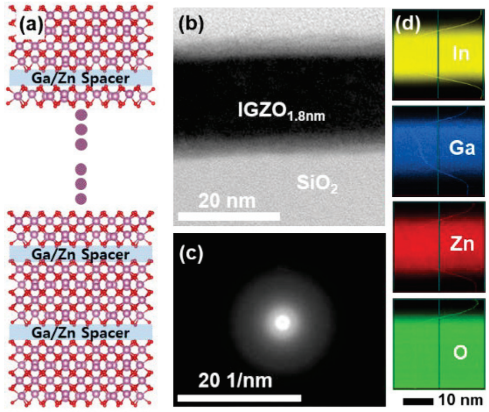

Figure 2. (a) Schematic diagram of the vertical structure of the PEALD-grown IGZO, (b) TEM image of an IGZO1.8nm thin film corresponding to (c) the selected area electron diffraction pattern, and (d) energy dispersive spectroscopy mapping of the elemental distributions of In, Ga, Zn, and O.

A photograph of a bottomgate top-contact-structured TFT fabricated on a PI substrate are shown in Figure 3. Figure 3 a,b exhibits representative transfer and output curves, respectively, of the flexible IGZO1.8nm TFT, showing a μ eff value of 47.9 ± 1.9 cm2/(Vs), Vth value of −2.3 ± 0.3 V, and S.S. value of 0.18 ± 0.05 V/dec. successful production of a flexible PEALD-grown IGZO TFT with a mobility value of ~50 cm2/(V s) indicates its potential for replacing low temperature polysilicon (LTPS) TFTs, since the application of the latter is limited by its high fabrication temperature.

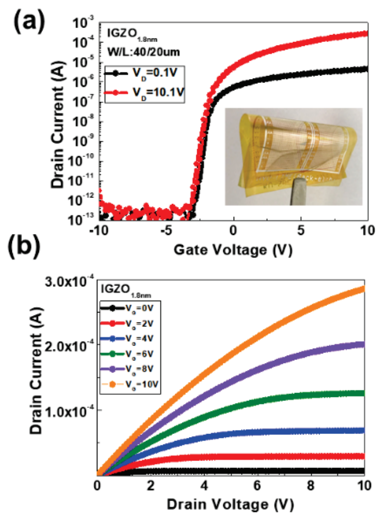

Figure 3. (a) representative transfer curve (inset: Photograph of devices fabricated on the PI substrate)

(b) output curve for a flexible PEALD-grown IGZO device with an active layer thickness of 1.8 mm.

SnO thin films were fabricated on glass substrates at 100 ^{o}C using 6-inch lateral gas flux thermal ALD. We held the chamber pressure at 300 mtorr with 50 sccm of N_2 purge gas. N,N'-tert-butyl-1,1-dimethylethylenediamine stannylene (II) and water were used as a precursor and reactant, respectively [5]. Inverted staggered SnO TFTs were fabricated on a p-silicon wafer with a thermally grown SiO_2 (100 nm) layer as a gate insulator. Every TFT had a 10 nm active layer thickness and thermal annealing was conducted before source/drain (S/D) deposition. 100 nm-thick of Mo metal was deposited to form the S/D electrode using magnetron sputtering. The channel was patterned and the width (W), length (L) were W = 40 μm and L = 20 μm, respectively. SnO TFT characteristics exhibited in Figure 4 a, with a ~10^{20} cm^{-3} high annealed at 400 ^{o}C. The on/off current ratio, field effect mobility (μ_{eff}) and sub-threshold swing (S.S) were 1.27×10^3, 0.98 cm^2/Vs and 5.7 V/decade, respectively. The on/off current ratio improved significantly after annealing at 400 ^{o}C. It is unclear why the off current decreases in the 400 ^{o}C annealed sample.

CuO_x films were grown using an ALD system at 100 °C. Hexafluoroacetyl-acetonateCu(I)(3,3-Dimethyl-1-butene)-((hfac)Cu(I)(DMB)) and ozone gas were used as the source of copper and oxygen, respectively. To fabricate bottom gate TFT structures, heavily doped p-silicon substrates were used as the gate metal, onto which 100 nm-thick silicon oxide (SiO_x) films were grown as the gate insulator. After depositing the CuO_x semiconductor, 50 nm-thick Au was deposited, followed by the deposition of a 20 nm- thick Ni layer to form the source-drain electrodes by shadow mask patterning. The final channel width and length of the devices were 1000 μm and 100 μm, respectively. Figure 4 b shows the transfer curves of the TFTs incorporating ALD CuO_x films deposited at 100 ^{o}C annealed at different temperatures [6]. The devices with CuOx annealed at 300 ^{o}C exhibits the highest field effect mobility (≈ 5.64 cm^2/V s) with a high on/off ratio (≈10^5), whereas the ones annealed at 200 and 400 ^{o}C have lower mobility (0.52 and 0.2cm^2/V s, respectively). The as-deposited CuO_x TFT exhibits relatively high off current levels and large subthreshold swing, which may result from a large density of defect states owing to the non-stoichiometry induced by the low deposition temperature. The devices annealed at 200 ^{o}C and 400 ^{o}C exhibit relatively poor performance compared to the as-deposited condition and the device annealed at 300 ^{o}C. The CuO_x film annealed at 200 ^{o}C results in low off current, showing that the active layer is semiconducting. it may be concluded that the high mobility of the CuO_x device annealed at 300 ^{o}C results from a moderate carrier concentration (relatively low portion of the CuO phase than when annealed at higher temperatures) and the preservation of the amorphous microstructure.

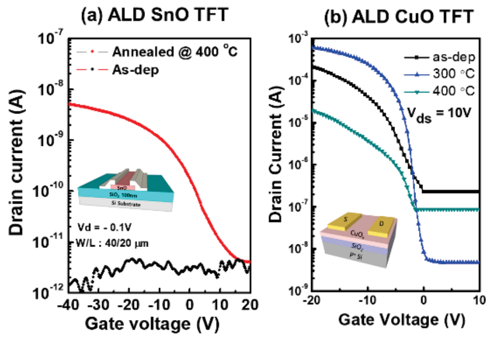

Figure 4. (a) Representative Transfer curve of ALD p-type SnO TFT with the field effect mobility of 0.98 cm^2/Vs at annealed 400^{o}C. (b) Representative Transfer curve of ALD p-type CuO TFT with the field effect mobility of 5.64 cm^2/Vs at annealed 350^{o}C.

4 CONCLUSIONS

ALD technique is the following key consequence such as 'self-limiting film growth': the same amount of films is deposited on all the surfaces irrespective of the dose of precursors/oxidants. This leads to several important practical advantages, like excellent conformality, uniformity over large areas, accurate film- thickness, simply composition-control and easy multi-composition growth. Currently, reactive sputtering method is cost-effective and well-established in Display industries, but it also has the significant limitations to improve oxide semiconductor TFT performances with various process variables. Although the commercial sputtering may overcome a few above issues, the demanding scale-down and ultrahigh-resolution will be challengeable. Although ALD has still the remaining issues before the practical production, the unique characteristics of ALD looks like nearly an ideal thin film deposition. Therefore, ALD will be one of important AOS processes to solve the limitations and open the possibility of new era in AOS applications.

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