Towards Monolithic Active Matrix Nanowire Light-Emitting Diodes

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ABSTRACT

Gallium Nitride (GaN) based light-emitting diodes (LEDs) are poised to be the next display technology. Though the conventional approach of a separately fabricated backplane adds cost. Here, a vertical monolithic approach is presented pairing an LED and transistor. An on/off current ratio over 10^4 is achieved with modulation demonstrated.

1 INTRODUCTION

Micro-LEDs (μ-LEDs) are emerging as the next generation of display technology over conventional liquid crystal displays (LCDs) or organic LED (OLED) displays. μ-LEDs offer a self-emissive display similar to OLED technologies, though without some of the processing drawbacks [1]. The movement towards μ-LEDs has been primarily driven by the high efficiency, long lifetime, and the promise of high pixel density [2-4]. Larger scale LEDs, in the range of hundreds of microns, are already commercially sold in applications such as home lighting, and is a well-developed technology [4]. Though LEDs are brought to the nanoscale in order to make high resolution displays. These LEDs are made from the III-Nitride materials system, which is distinct from silicon where conventional complementary metal oxide semiconductor (CMOS) circuits are made. The III-Nitride materials system is also distinct from glass, where silicon thin-film transistors (TFTs) are fabricated for use with LCD and OLED technologies. In either case, the controlling TFT or CMOS transistor backplane has typically been separately fabricated then connected with either the individual LEDs or entire LED wafer to create a μ-LED display. Though ultimately, having separate fabrication of the LEDs and transistor backplane increases costs, adds process complexity, and can negatively impact pixel density.

To address this limiting issue, a novel monolithic approach is utilized in order to reduce costs, decrease process complexity, and increase pixel density. This is done through fabricating the transistor backplane in the same III-Nitride materials system, without use of separate manufacturing or growth techniques. In this work, a vertical LED is paired with a vertical gate-all-around (GAA) transistor to provide control over the LED. The arrangement of the two devices is shown in Fig. 1, where the LED is in series with the transistor.

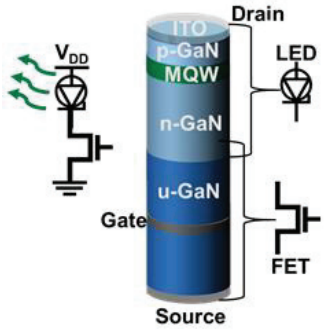

Fig. 1 Vertical Nanowire LED integrated with a FET

This integration between the two components is a critical part of an active matrix design, where the driving transistor is in series with the LED to control the current flow and corresponding brightness levels. The type of transistor initially utilized here is a static induction transistor (SIT) [5]. An SIT makes use of an n-i-n structure with a schottky gate, allowing a simple fabrication flow. An n-i-n structure is natively present on conventionally grown LED wafers, where the n-GaN region for the LED can serve as both the drain of the transistor and the cathode for the LED. The intrinsic, or slightly n-type, channel region of the transistor can be the buffer region of the LED. The source of the transistor can be the thin region close to the sapphire substrate where O_2 and other defects incorporate, leading to an n-type layer [6-8]. These identified layers are made use of for these initial device results, though alternative types of transistors and doping schemes can also be utilized in the realization of this vertical integration.

For an SIT a short gate length is employed, where the punch-through phenomena is capitalized upon for switching performance. The SIT produces triode-like instead of the saturating pentode-like behavior of conventional transistors such as the metal oxide semiconductor field effect transistor (MOSFET).

The work presented here makes use of a top-down fabrication approach, as opposed to bottom up growth, with the use of conventionally grown LED wafers. Making

use of vertical devices allows increased resolution for displays, with minimal area consumed on the wafer.

2 DEVICE FABRICATION

These vertical devices can be either fabricated in a high aspect ratio nanowire format or a low aspect ratio planar architecture. Results of the nanowire work are presented and discussed here.

A conventional InGaN/GaN green LED grown by metal organic chemical vapor deposition (MOCVD) on a sapphire wafer is used and demonstrated in this work. To begin, Ni or SiO_2 nano-dots are patterned on the surface of the wafer to act as the hard mask for the nanowire etch, Fig 2(a). A chlorine based reactive ion etch (RIE) is performed to etch the nanowires, stopping at an area close to the substrate for the later source contact. After the nanowires are etched, a hydroxyl based wet etch is done to reveal the m-plane, making the wires perfectly vertical and removing any etch induced damage [9].

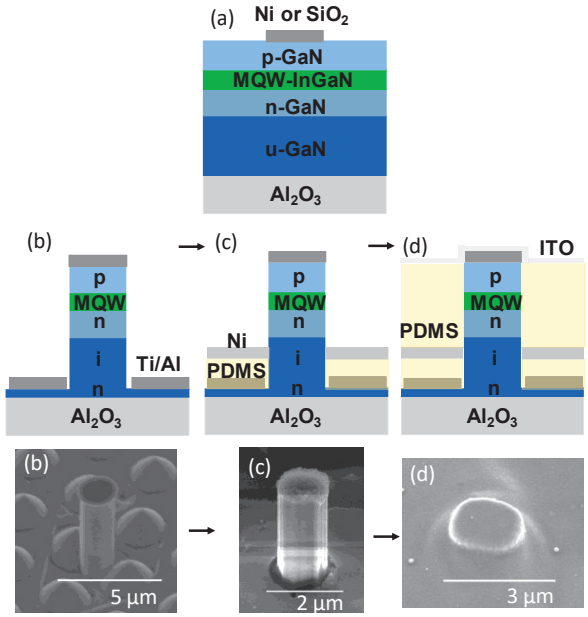

Fig. 2 (a) Growth structure with hard mask, (b) Nanowire etch and source metal, (c) PDMS etch-back and gate metal, (d) PDMS etch-back and ITO deposition

Once the wires are formed, a layer by layer fabrication process is performed in order to build up the metal and insulator layers to complete the device. This unique layer by layer fabrication process is also compatible with wires that are grown, instead of formed through a top down etch. The source contact for the SIT is formed through a directional metal deposition and lift-off step. Ti and Al are directionally evaporated, and patterned through a photoresist lift-off step, Fig. 2(b), leaving metal on the top and base of the wires. A directional evaporation is critical, as deposition on the sidewalls of the nanowires can lead to an electrical short. After lift-off, the sample is annealed at 900°C in a nitrogen atmosphere, in order to from an ohmic contact. During the high temperature anneal, the Ti bonds with N in the material, forming TiN and generating N vacancies which act as donors, further transforming the base of the nanowires into an n-type region [10-11].

Polydimethylsiloxane (PDMS) is then spin coated thick and etched back to act as a spacer between the source and gate metals. PDMS is used as the interlayer dielectric, due to the planarization properties of the material and the wet chemical inertness during processing. Though ultimately, SiO_2 combined with a chemical mechanical polishing (CMP) step, represent a more manufacturable alternative.

Following the PDMS dielectric coat and etch back, 40 nm of Ni is directionally evaporated and subsequently lifted off, forming the gate, Fig 2(c). Due to the layer by layer fabrication approach utilized, the deposition thickness controls the gate length, allowing finer dimensions than photolithography. This makes possible the realization of a 40 nm gate length device, while still making use of older g-line or i-line steppers for fabrication. Additional PDMS is next coated and etched back to reveal just the tips of the nanowires for the source contact metallization. Excessive etching at this stage can lead to later electrical shorting during the metallization. Next, transparent indium tin oxide (ITO) is deposited through sputtering to coat the surface, Fig 2(d). Patterning and wet etching are performed to pattern the ITO. Final contact cuts are made in the PDMS in order to open windows in the dielectric for electrical probing.

The approach outlined through this fabrication makes large scale arrays of nanowire devices possible to form, Fig. 3, while sacrificing minimal area on the wafer.

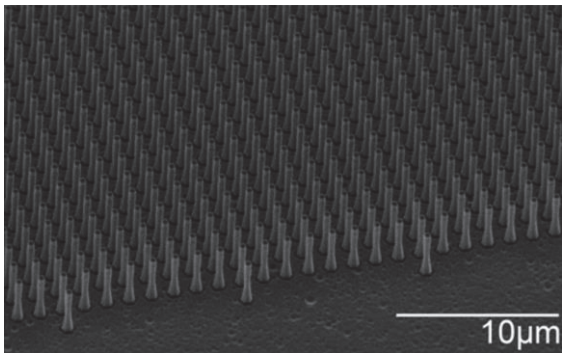

Fig. 3 Nanowire array post-etch, patterned through e-beam lithography

3 RESULTS AND DISCUSSIONS

Both electrical and optical characterization have been performed on these devices. Results are shown for devices with an average of 45 wires in parallel, with nanowire diameters of 900 nm.

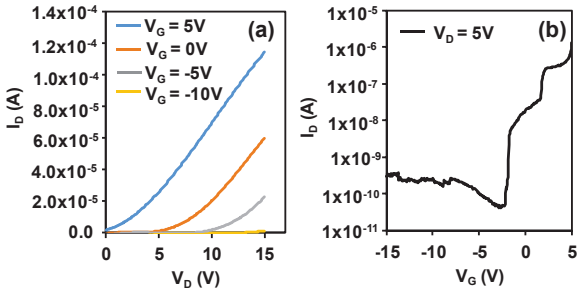

Fig. 4 (a)I_D-V_D family of curves, (b) I_D-V_G on/off

The measured I-V results are shown by Fig. 4. The family of curves, Fig. 4(a), shows triode-like or non-saturating behavior over the conventional pentode-like or saturating behavior of a MOSFET. The non-saturating behavior arises from the gate punch-through effect, which is a short-channel effect in a MOSFET to be avoided. In the case of an SIT, punch-through is purposely exploited. The unique non-saturating behavior of an SIT could be beneficial for LED brightness control. The characteristics in Fig. 4(a) also demonstrate normally on performance, with current pinch-off at negative biases. Fig. 4(b) shows the on/off current ratio over 10^4 at a drain bias of 5 V. It is seen that the device fully turns off at -2.2 V. With a positive gate bias above ~2.5 V, the Schottky gate turns on and unwanted gate current dominates. The mechanisms behind the device operation are shown in Fig. 5. Depletion regions are formed by the gate metal, where the steady state depletion width depends primarily on the doping and metal work function. As a reverse bias is applied the depletion regions extend, pinching off the vertical current flow.

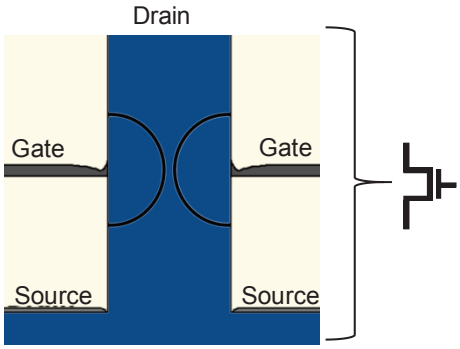

Fig. 5 SIT cross-section illustrating depletion regions

If enhancement mode operation with positive threshold voltages is desired, merging the depletion regions through shrinking the diameter can be utilized. Fig. 6(a) shows the Silvaco Atlas simulated I_D-V_G performance when the diameter of the nanowire is reduced to 300 nm. The corresponding threshold voltage is found to increase from -2.2 V to around 0.5 V. With a reduced diameter the gate leakage is also reduced when operating with positive gate biases. Fig. 6(b) shows the corresponding energy bands taken from a lateral cross section of the 300 nm device, where at 3 V the gate diode is not still not on due to the present of an electron barrier height. Alternatively, to achieve enhancement mode operation, design of an n-p-n structure intrinsically allows positive thresholds, while use of a MOSFET design can be chosen to eliminate gate leakage.

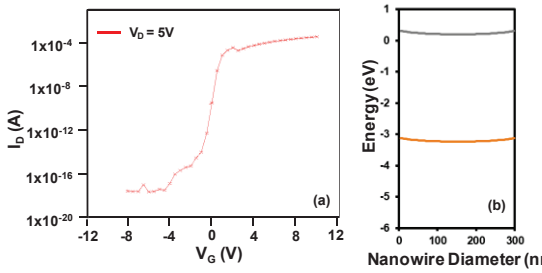

Fig. 6 (a) Simulated I_D-V_G for 300 nm, (b) Simulated Energy band bending at 3 V for 300 nm

The optical results are recorded and shown in Fig. 7. Electroluminescent (EL) data is captured through a spectrometer, holding the LED voltage constant and varying the gate bias. Due to the depletion mode operation of an SIT, light is observed with 0 V applied to the gate. The intensity can be increased with application of a positive gate bias. With negative gate biases, the intensity decreases, until the SIT fully pinches the current off. These optical results match with the recorded I-V data, where at -10 V to the gate, the current is fully pinched off.

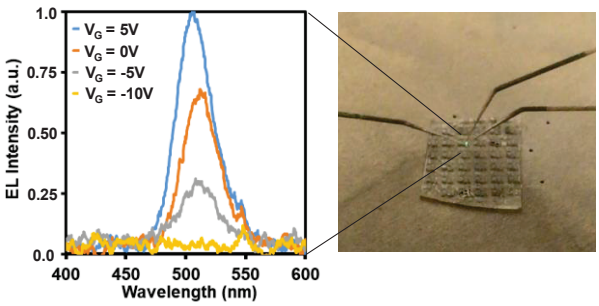

Fig. 7 EL data with varying gate bias

The recorded results demonstrate the ability of the transistor to control and modulate current flow through the LED. This control can allow for the application of rapid switching or brightness modulation which are critical requirements for μ-LED displays.

4 CONCLUSIONS

Vertically integrated LED-FETs were fabricated and explored. Electrical, optical, and simulation results are all presented to explore the device operation. It is found that vertical integration of an LED and SIT present a means to successfully control current flow and light emission, finding an on/off current ratio of 10^4. The device was recorded to fully turn off the LED at a gate bias of -10 V

through both the I-V and EL data. A method to introduce enhancement mode operation is discussed, where diameter reduction can be done if an n-i-n structure is utilized. This work can open the door to reduced fabrication costs and higher pixel densities for μ-LED displays.

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