

Hydrogen-Treated Stable IGZO Thin-Film Transistor with All-Sputtered Gate Stack

Taewon Seo, Juyoung Yun, Suwon Seong, Hyuk Park, Gilsu Jeon, and Yoonyoung Chung*

y chung@postech.ac.kr

Electrical Engineering, POSTECH, Korea

Keywords: IGZO TFT; hydrogen plasma; interface; stability

ABSTRACT

a-IGZO contains numerous defects, which degrade the performance and stability of thin-film transistors. Especially, the interface traps have dominant effects on the device properties, such as hysteresis and carrier scattering. We demonstrated highly-stable *a*-IGZO TFT with all-sputtered gate stack. Outstanding interface properties were obtained by passivation with hydrogen plasma treatment.

1 INTRODUCTION

Amorphous In-Ga-Zn-O (*a*-IGZO) has attracted much attention as the next-generation semiconductor material due to its high mobility in non-crystalline phase, outstanding uniformity, low process temperature, high transparency, and process compatibility with conventional semiconductor products [1-3]. However, *a*-IGZO thin-film transistors (TFTs) have a critical issue with the stability because the amorphous thin film contains numerous defects. Especially, the interface traps have more dominant effects on the device performance compared to the bulk traps, so the interface between semiconductor and dielectric must be treated carefully [4].

Conventionally, silicon dioxide (SiO₂) deposited by plasma-enhanced chemical vapor deposition (PECVD) has been widely adopted as the gate dielectric of *a*-IGZO TFTs. However, CVD has a disadvantage of high cost, and PECVD is known to induce high interface traps, which degrade the device reliability [5]. High-*k* dielectrics, such as Al₂O₃, HfO₂, and TiO₂, have been suggested as alternatives for PECVD-grown SiO₂ [6-8]; however, their quality is not yet enough to compete with the conventional approach. In this study, we demonstrated highly-stable *a*-IGZO TFTs with SiO₂ gate dielectric deposited by a versatile sputtering method. Sputtered gate dielectrics generally exhibit poor qualities with large trap density [9]. We utilized hydrogen plasma treatment to reduce the defects in as-sputtered thin films and confirmed an effective trap passivation from the improved electrical properties of TFTs.

2 EXPERIMENT

A quartz substrate was cleaned by acetone and isopropyl alcohol. An aluminium layer (100 nm) was sputtered for gate electrode. A SiO₂ thin film (30 nm) was deposited by RF magnetron sputtering and used as the gate dielectric. A hydrogen plasma treatment was performed for 50 secs with RF power of 250 W and hydrogen pressure of 50 mTorr at 250 °C. An *a*-IGZO layer (30 nm) was sputtered at room temperature with 120 W RF power at 5 mTorr Ar pressure. The sample was then annealed in O₂ ambient at 300 °C for 120 mins. A bilayer of molybdenum and aluminium (5/100 nm) was used for source and drain electrodes. All the layers were patterned by a standard photolithography process.

3 RESULTS and DISCUSSION

The schematic of *a*-IGZO TFTs fabricated with sputtered gate dielectric (SiO₂, 30 nm) is shown in Fig. 1. During I-V measurements, the gate bias was swept from -5 to 10 V and then reversely swept back to -5 V to check the hysteresis.

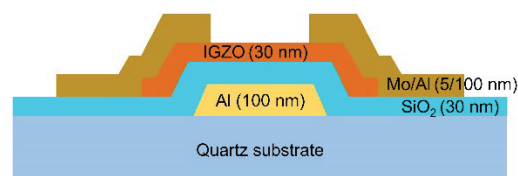


Fig. 1 Schematic of IGZO TFT in this study.

I_D-V_{GS} curves of *a*-IGZO TFTs with and without the hydrogen treatment are shown in Fig. 2. The gate leakage current of both TFTs was under 1 pA at V_{GS} = 10 V. The bare sample had the field-effect mobility of 12.62 (±0.23) cm²V⁻¹s⁻¹ and the subthreshold swing (SS) of 0.13 V/dec. In hydrogen-plasma-treated TFTs, the field-effect mobility and the SS were slightly improved: 13.43 (±0.17) cm²V⁻¹s⁻¹ and 0.11 V/dec. There was no difference in the threshold voltage of both samples. A significant improvement was observed in the hysteresis characteristics with hydrogen-plasma-treated TFTs. A large hysteresis of 0.5 V was observed in the untreated

samples, while the hydrogen-treated samples exhibited the same forward/reverse I-V data. Hydrogens are known to passivate the interface traps associated with oxygen interstitials (Fig. 3) [10, 11]. As a result, the hydrogen plasma enhances the electrical properties of a-IGZO TFTs.

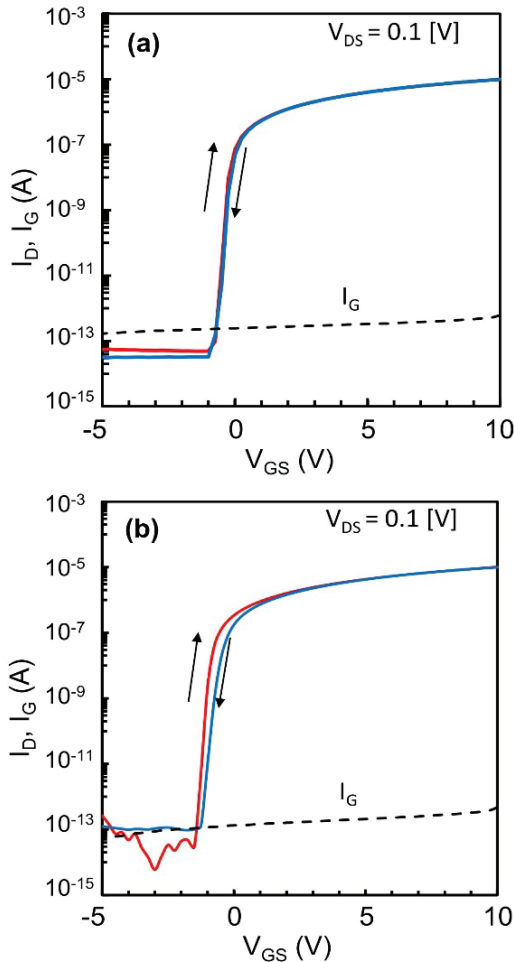


Fig. 2 I_D - V_{GS} curves of IGZO TFT (a) with and (b) without hydrogen plasma treatment. The hysteresis was effectively diminished in the hydrogen-treated samples.

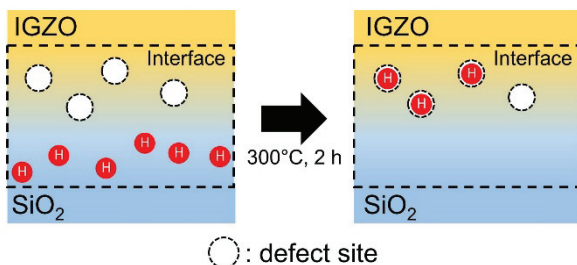


Fig. 3 Schematic of hydrogen treatment effect at the a-IGZO/SiO₂ interface. Hydrogen atoms diffuse from SiO₂ to a-IGZO during annealing process and combine with defect sites to form stable states.

We measured the stability of hydrogen-treated TFTs under a positive bias stress (PBS) condition by applying a gate field of 1.7 MV/cm for 3,600 secs. In Fig. 4, the threshold voltage of the TFTs was shifted by only 0.29 V, which is outstanding compared to the previous studies with similar e-field stress [10, 12, 13]. These outstanding hysteresis and stability characteristics with sputtered gate dielectric are attributed to the reduced interface traps by hydrogen passivation [10, 11].

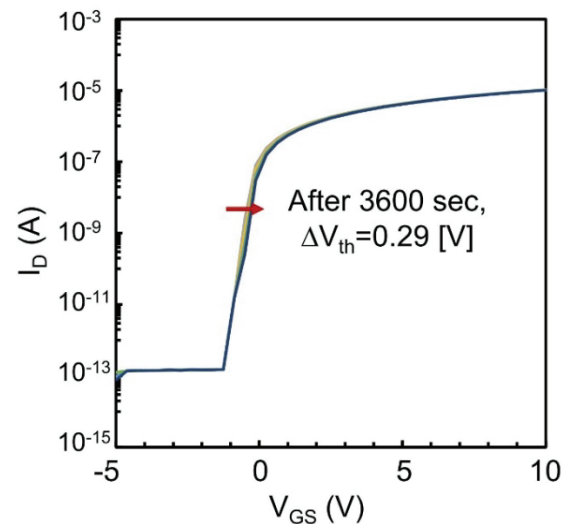


Fig. 4 I_D - V_{GS} curves of IGZO TFT with hydrogen treatment under PBS condition. With 1.7 MV/cm stress for 3,600 s, the threshold voltage shift was less than 0.3 V.

4 CONCLUSIONS

In summary, we successfully achieved outstanding interface properties between a-IGZO and SiO₂, all deposited by versatile sputtering. The TFT characteristics, such as field-effect mobility and SS, were enhanced by hydrogen plasma treatment. Due to the effective passivation of interface traps by hydrogen atoms, a hysteresis was removed in IV data, and the threshold voltage was shifted by only 0.29 V after a PBS under 1.7 MV/cm for 3,600 secs.

REFERENCES

- [1] Y. Kuo, "Metal Oxide High-k Thin Films - from Gate Dielectrics to Nonvolatile Memories to LEDs," *Ecs Transactions*, vol. 54, no. 1, pp. 273-281, (2013).
- [2] H. N. Lee *et al.*, "Oxide TFT with multilayer gate insulator for backplane of AMOLED device," (in English), *J Soc Inf Display*, vol. 16, no. 2, pp. 265-272, Feb (2008).

- [3] K. Nomura, H. Ohta, A. Takagi, T. Kamiya, M. Hirano, and H. Hosono, "Room-temperature fabrication of transparent flexible thin-film transistors using amorphous oxide semiconductors", *Nature*, vol. 432, no. 7016, pp. 488-492, (2004).
- [4] B. Kim, E. Chong, D. Hyung Kim, Y. Woo Jeon, D. Hwan Kim, and S. Yeol Lee, "Origin of threshold voltage shift by interfacial trap density in amorphous InGaZnO thin film transistor under temperature induced stress," *Applied Physics Letters*, vol. 99, no. 6, p. 062108, (2011).
- [5] T. Kawamura *et al.*, "1.5-V operating fully-depleted amorphous oxide thin film transistors achieved by 63-mV/dec subthreshold slope," in *2008 IEEE International Electron Devices Meeting*, pp. 1-4 (2008).
- [6] J.-S. Park, J. K. Jeong, Y.-G. Mo, and S. Kim, "Impact of high-k TiO₂ dielectric on device performance of indium-gallium-zinc oxide transistors," *Applied Physics Letters*, vol. 94, no. 4, p. 042105, (2009).
- [7] J. C. Park *et al.*, "Impact of high-k HfO₂ dielectric on the low-frequency noise behaviors in amorphous InGaZnO thin film transistors," *Japanese Journal of Applied Physics*, vol. 49, no. 10R, p. 100205, (2010).
- [8] P. Ma *et al.*, "Low voltage operation of IGZO thin film transistors enabled by ultrathin Al₂O₃ gate dielectric," *Applied Physics Letters*, vol. 112, no. 2, p. 023501, (2018).
- [9] W. Choi, C. Choo, and Y. Lu, "Electrical characterization of rapid thermal annealed radio frequency sputtered silicon oxide films," *Journal of applied physics*, vol. 80, no. 10, pp. 5837-5842, (1996).
- [10] J. Sheng, J.-H. Han, W.-H. Choi, J. Park, and J.-S. Park, "Performance and stability enhancement of In-Sn-Zn-O TFTs using SiO₂ gate dielectrics grown by low temperature atomic layer deposition," *ACS applied materials & interfaces*, vol. 9, no. 49, pp. 42928-42934, (2017).
- [11] T. Kim, Y. Nam, J. Hur, S.-H. K. Park, and S. Jeon, "The influence of hydrogen on defects of In-Ga-Zn-O semiconductor thin-film transistors with atomic-layer deposition of Al₂O₃," *IEEE Electron Device Letters*, vol. 37, no. 9, pp. 1131-1134, (2016).
- [12] J. K. Jeong, H. Won Yang, J. H. Jeong, Y.-G. Mo, and H. D. Kim, "Origin of threshold voltage instability in indium-gallium-zinc oxide thin film transistors," *Applied Physics Letters*, vol. 93, no. 12, p. 123508, (2008).
- [13] A. Kiazadeh *et al.*, "Improving positive and negative bias illumination stress stability in parylene passivated IGZO transistors," *Applied Physics Letters*, vol. 109, no. 5, p. 051606, (2016).