

A Gate Driver Circuit Integrating in a 15-inch AMOLED Display Based On IGZO-TFTs

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Abstract

A depletion-mode indium-gallium-zinc-oxide thin-film-transistor (IGZO-TFT) gate driver on array (GOA) integrated circuit has been proposed. IGZO-TFTs are turned off completely due to the introduction of series-connected two-transistor structure and dual low-voltage-level power signal. Finally, the GOA circuit was placed in a 31-inch AMOLED display to testify the function.

1. Introduction

Recently, active matrix organic light-emitting diode (AMOLED) displays have become one of the most promising techniques for TV displays, wearable displays, mobile phones and flexible smart devices [1-2]. In order to decrease production cost, gate driver on array (GOA) has become a main driving technique instead of gate IC. Moreover, GOA offers narrow bezel for displays [3]. For example, in our previous study, GOA was placed at the placed at the bottom side of display, the structure of which contributed significantly to border reduction and a narrow border width of 1mm was obtained.

It is well known that three common thin-film transistors (TFTs) structures have been explored for display manufacturing, such as amorphous silicon (a-si) TFTs [4], low temperature poly-Si (LTPS) TFTs [5] and amorphous indium-gallium-zinc oxide (a-IGZO) TFTs [6]. Due to their low mobility, the utilization of a-Si TFTs is mainly focused on the field of liquid crystal display. Since the uniformity of LTPS films is poor, the use of LTPS-TFTs is limited to AMOLED display with small size. IGZO-TFTs have achieved mass production target in the field of AMOLED displays with large size because of their high mobility ($1\sim 100\text{ cm}^2/\text{V}\cdot\text{s}$) and good uniformity [7-10].

It is well known that IGZO-TFTs often act as depletion-mode device. It should be noted that some structures, such as series two transistors structure (STT) and dual low power system (Dual-VGL), are widely used to reduce leakage current from TFTs. Therefore, IGZO-GOA circuit is much more complicated than a-Si GOA and LTPS-GOA circuit. In this work, we design a stable GOA circuit. In order to test GOA function, GOA was placed in a 15-inch AMOLED display with a resolution of FHD (1920×1080) and the waveforms of GOA were measured through oscilloscope.

2. TFT Introduction

Top gate (TG) TFTs have been designed for GOA circuits and the cross-sectional diagram of TG-TFT is demonstrated in Fig.1. TFT was fabricated according to the followings: A SiO_x buffer layer was deposited by plasma enhanced chemical vapor deposition (PECVD) as a dielectric layer. Subsequently, IGZO active layer was deposited and patterned on buffer layer by wet etching. Then gate isolation layer (GI) and gate electrode (G) were subsequently deposited on IGZO layer. In the next step, SiO_x was deposited by PECVD for top gate insulator (ILD), followed by deposition of a Mo layer as source/drain electrodes for TFTs. Finally, a SiO_x layer was deposited as a passivation of top-gate a-IGZO TFTs.

The transfer and output curves of IGZO-TFT with the size of $W/L=10\mu\text{m}/8\mu\text{m}$ recorded by a Keithley-4200 SCS semiconductor parameter analyzer is demonstrated in Fig.2. This TFT exhibits good switching performance with threshold voltage of -1.8V, indicating depletion mode characterization of device. Fig.2 (b) shows the output characteristics (I_d - V_d) of the TFT device ($W/L=10\mu\text{m}/8\mu\text{m}$) for V_{gs} varying from 0.1 V to 25.1 V. As shown, the I_{ds} value increases with V_{gs} value. The uniformity research result of IGZO-TFT with TFT size of $W/L=10\mu\text{m}/10\mu\text{m}$ over the whole glass (G4.5 glass, 730mm×920mm) is shown Fig.3. It can be seen that V_{th} , which varies from -1.8V to -0.5V, demonstrates high uniformity over this glass.

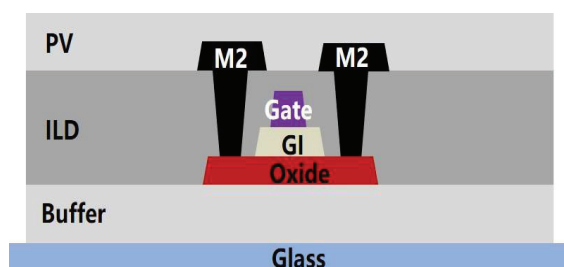


Fig.1. Cross-sectional diagram of TFT structure

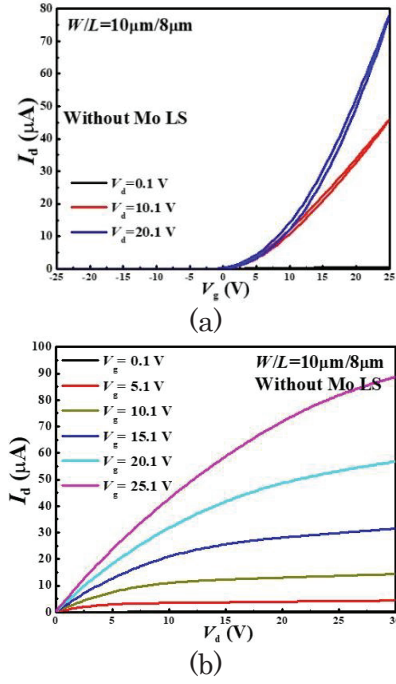


Fig.2. (a) Transfer and (b) output characteristic curves of a-IGZO TFT

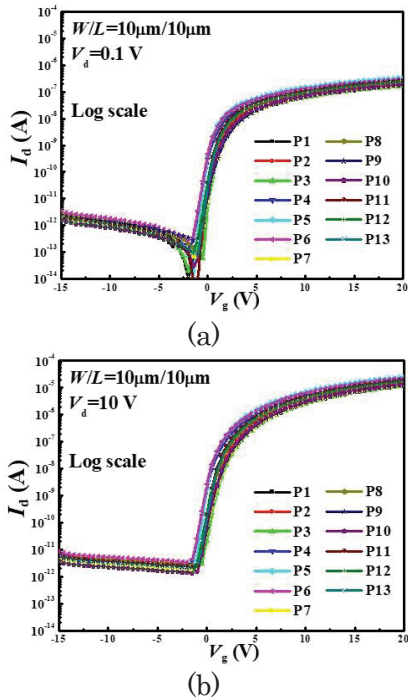


Fig.3. Uniform research of (a) transfer characteristic curves of a-IGZO TFT over whole glass

3. GOA Circuit

Fig.4a exhibits the schematic of convenient GOA circuit with traditional top gate TFT structure, which is composed of a pull-up unit (T8, T10), pull-up control unit (T1a, T1b), reverse unit (T4, T50, T5E, T60, T6E, T70, T7E), pull-down holding unit (T90, T9E, T110, T11E), pull-down unit (T2a, T2b) and feedback unit (T1C, T2C, T3). In order to increase the reliability of GOA, two group of pull-down

holding unit is utilized in GOA alternately. The corresponding waveforms of GOA can be seen in Fig.4b. Fig.5 shows the block system of the proposed gate driver circuit with 1080 stairs.

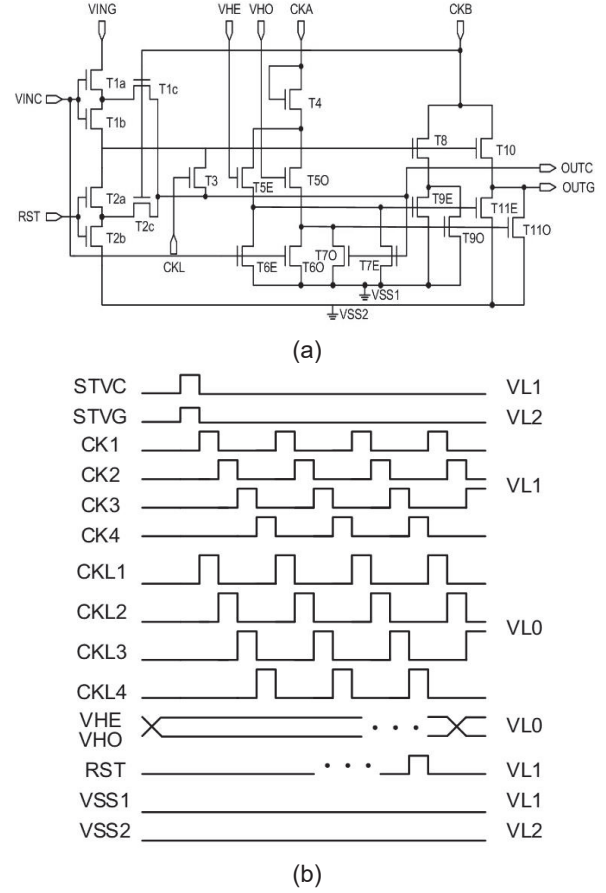


Fig.4. Schematic diagram of (a)GOA circuit; (b) operation waveforms of the proposed integrated GOA circuit

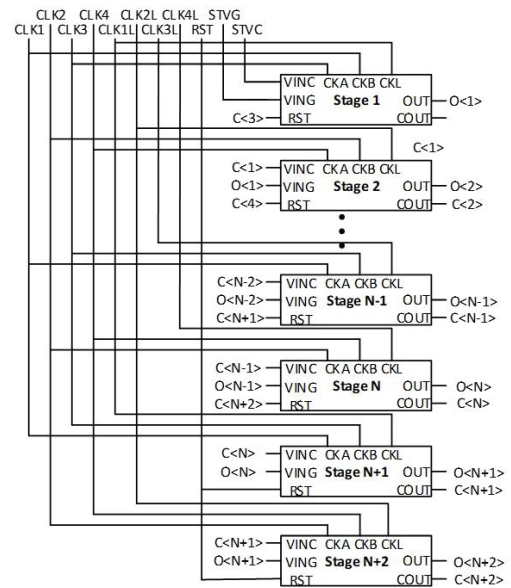


Fig.5. Block diagram and connections between stages of the proposed GOA circuit

Fig. 6(a) indicates the comparison between the experimental and simulated I-V characteristics of IGZO-TFT with W/L=10 μ m/8 μ m for T51 and T52. It can be seen that the experimental and simulated results are matched. The voltage amplitudes of input signals can be seen in Tab.1. Fig.7 illustrates the simulated Out(n) waveforms of the proposed circuit from the first stage to the 48th stage. Sequential pulse signals, indicative of the output function of the proposed GOA circuit, have been successfully observed.

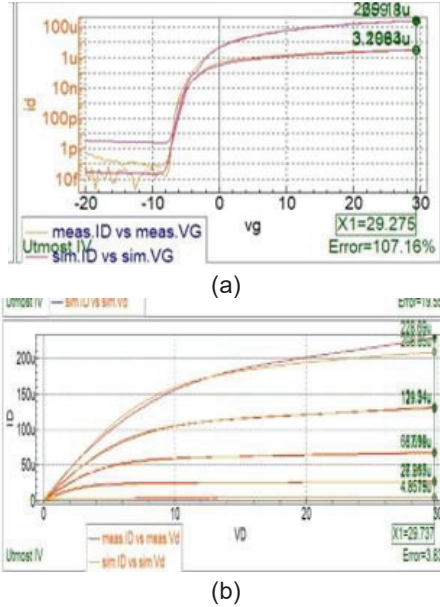


Fig.6. Measured and simulated transfer curves of TFT

Tab.1 The voltage amplitude of input signals

Items	GOA Signal	Voltage range				Items	GOA Signal	Voltage range			
		min. (V)	max. (V)					min. (V)	max. (V)		
1	STVC	-10	VGL1	+20	VGH	2	STVG	-5	VGL2	+20	VGH
3	CK1	-10	VGL1	+20	VGH	4	CK2	-10	VGL1	+20	VGH
5	CK3	-10	VGL1	+20	VGH	6	CK4	-10	VGL1	+20	VGH
7	CKL1	-15	VGL0	+20	VGH	8	CKL2	-15	VGL0	+20	VGH
9	CKL3	-15	VGL0	+20	VGH	10	CKL4	-15	VGL0	+20	VGH
11	VHE	-15	VGL1	+20	VGH	12	VHO	-15	VGL1	+20	VGH
13	VSS1	-10V			VGL1	14	VSS2	-5V			VGL2
15	RST	-10	VGL1	+20	VGH						

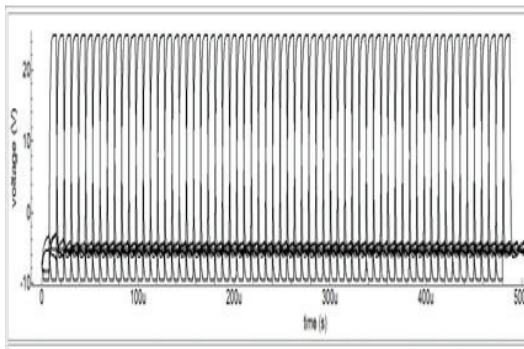


Fig.7. The output signals of GOA circuit simulated by Spice from stage1 to 48

Fig.8 displays the simulated output waveforms of 1080th stair in GOA circuit as a function of TFT threshold voltage shift (V_{shift}). The transformation from pulse waveform to distorted waveform occurred at a critical threshold voltage of -4V and 12V. In other words, the GOA circuit can function well within a V_{shift} margin of -4~12V, indicative of a broad V_{shift} margin window

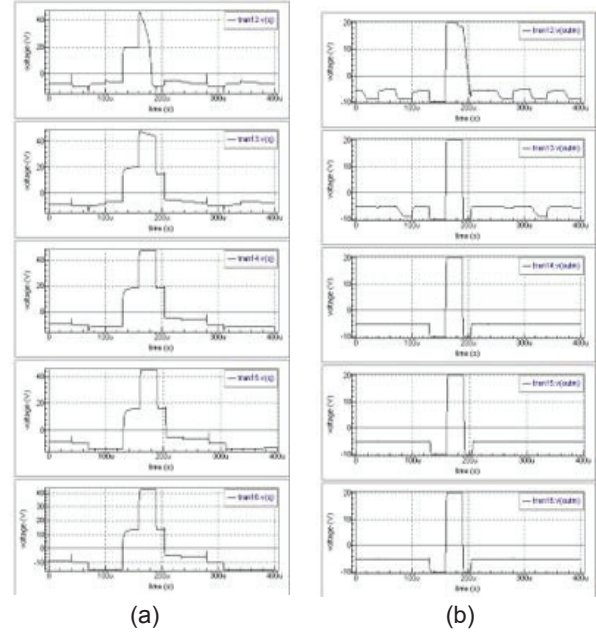


Fig.8. The V_{shift} margin of the GOA circuit: (a) negative direction; (b) positive direction

4. Experimental results

The optical image of GOA can be seen in Fig.9. Subsequently, to testify the GOA circuit, output signals of the GOA circuit are characterized by an oscilloscope. Fig. 10 displays the pictures of 5th and 40th output pulse with a frame of 60HZ. As shown in measurement waveform of the proposed gate driver, the output waveforms are smooth and clear without any distortion. Fig.11 shows a photograph of display image of 15-inch AMOLED display, which is driven by the GOA circuit above. This picture demonstrates that the GOA circuit functions well in this display.

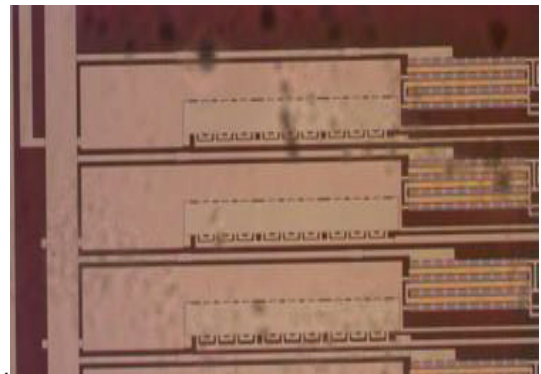


Fig.9. The border width of AMOLED display with (a) 18T1C GOA; (b) 6T1C GOA

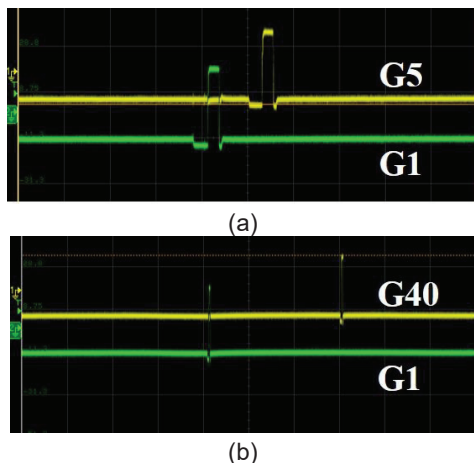


Fig.10. Measured output signals of GOA: (a) G5;(b)G40

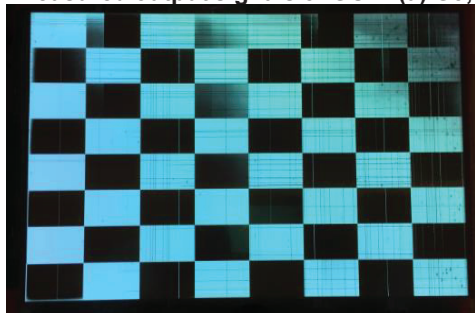


Fig.11. A photograph of this 15-inch AMOLED display driven by GOA

5. Conclusion

We have demonstrated a GOA circuit for a 15-inch AMOLED display. The proposed GOA circuit requires 20 TFTs for each stage. The simulated and experimental results have shown that the proposed GOA circuit can function well. This offers a high-quality gate drive circuit for AMOLED display.

Acknowledgment

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