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Design of Double-gate Organic Transistors with Tunable Threshold Voltage

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Abstract

We exploit a solid-liquid dual-gate organic transistor structure, where the threshold voltage of the liquid-gated conduction channel is controlled by an additional gate that is separated from the channel by a metal oxide gate dielectric. With this design the threshold voltage of the "sensing channel" can be linearly tuned in a voltage window exceeding 0.4 V. In general, the capability of tuning the optimal sensing bias will not only improve the device performance but also broaden the material selection for display devices.

1 INTRODUCTION

In recent years, thin film transistors (TFT) based on organic materials have attracted more and more attentions in display market due to the low-temperature processing and low off-state current and low voltage operation[1]. EGOFETs possess high sensitivity to the electrostatic potential variation at the interface of the organic semiconductor and the liquid electrolyte, where most sensing events take place. In this device structure, the electrical double layer formed at the solid-liquid interface enables fast device response and low voltage operation. OECT, on the other hand, delivers large transconductance ($gm=dI_D/dV_G$) through electrochemical doping induced by ion diffusion into the bulk semiconductor.[2] In many display-based applications, the operation voltage of the device should be kept low to reduce the power consumption.

In this work, we reduced the operation voltage of organic thin film transistors by designing a solid-liquid dual-gate organic transistor structure. In this device structure, the threshold voltage of the liquid-gated conduction channel is controlled by an additional gate that is separated from the channel by a metal oxide gate dielectric. We have demonstrated that with this design the threshold voltage can be linearly tuned in a voltage window exceeding 0.4 V. The dual-gate design can also be extended to accumulation-mode OECT structures, enabling tuning of the maximum transconductance point to below 0.3 V.

2 EXPERIMENT

Device Fabrication. The syntheses of g2T-T and DPP-DTT have been reported in Ref.3 and 4, respectively. Both the DG-OFET and DG-OECT exploit a heavily n-doped silicon wafer as the bottom gate electrode, on top of which a 50 nm thick Al_2O_3 layer was grown using atomic layer deposition (ALD) at a growth temperature of 200 ℃. A thin layer (~10 nm) of SiO_2 was then sputtered on top of Al2O3 with an Anatech Magnetron Sputtering Machine in RF mode under 100 ℃ for 10 min to form the bilayer bottom gate dielectric. Gold source and drain electrodes with a thickness of 30 nm were patterned by photolithography, yielding an interdigital structure of W:L=10×1000 μm: 40 μm. The oxide dielectric layers were passivated by immersing in 5 mM solution of OTS-8 in toluene for 24 h. After sonicated in toluene and dried with nitrogen gas, the substrates with gold electrodes were immersed in 10 mM 1-octanethiol solution in IPA for 2 min. The semiconducting layers of the OFET and OECT were formed by spin-coating the DPP-DTT solution in 1, 2-dichlorobenzene and the g2T-T solution in chloroform, respectively. A physiological saline solution, used as the electrolyte, was confined above the active area by a cylindrical polydimethylsiloxane (PDMS) reservoir with a radius of 1 mm. Finally, the dual-gate devices were completed by immersing the Ag/AgCl reference electrode into the electrolyte, serving as the top gate.

Device Characterization. Current-voltage characteristics were measured using a Keithley 2612B dual-channel system sourcemeter. Capacitance-voltage characteristics and cyclic voltammetry are measured with an impedance analyzer, Biologic SP-200, in a two electrodes configuration. The source and drain electrodes were shorted and connected to the counter electrode. The working electrode was connected to the top gate. A Keithley 2400 sourcemeter was used to apply voltage to the bottom gate in I-V and cyclic voltammetry measurements.

3 RESULTS AND DISCUSSION

Figure 1 shows the device structures developed in this study. For the dual-gate organic field-effect transistor (DG-OFET) we used a high crystallinity copolymer, poly (N-alkyl diketopyrrolo-pyrrole-dithienylthieno[3,2-b]thiophene) (DPP-DTT), as the semiconducting material; while for the dual-gate OECT (DG-OECT) device we applied the semiconducting polymer poly(2,5-bis(3-triethyleneglycoloxythiophen-2-yl)-co-thiophene) g2T-T, with hydrophilic side chains, as the active material. In the dual-gate design, an aluminum oxide (Al_2O_3, 60 nm) / silicon oxide (SiO_2, 8 nm) dielectric bilayer was employed to support the bottom-gate operation. The Al_2O_3 layer, formed through atomic layer deposition (ALD), was chosen due to its high dielectric constant of 8.9, allowing low voltage operation. A thin layer of SiO_2 was sputtered on top of the Al_2O_3 layer to facilitate the growth of an octyltrichlorosilane (OTS-8) self-assembled monolayer on the oxide surface, a modification process that is commonly used to reduce surface traps and improve the interface morphology for OFETs. For the top gate, a physiological saline solution (confined in a PDMS dwell) was used as the electrolyte and a Ag/AgCl reference electrode, immersed in the solution, was used as the gate electrode. In order to induce coupling between the top and bottom gate fields while maintaining efficient charge transport, the thickness of the semiconductor layer should be carefully tuned. We found that the optimal semiconductor thicknesses for the DG-OFET and DG-OECT structures are around 30 nm and 40 nm, respectively, which yield high field-effect mobility while at the same time allowing strong dual-gate effect.

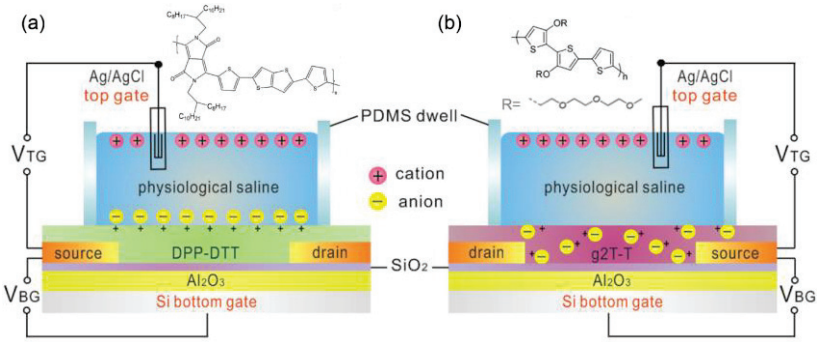

Figure 1. (a) Schematic cross-section of a DG-OFET device and chemical structure of DPP-DTT; (b) Schematic cross-section of a DG-OECT device and chemical structure of g2T-T.

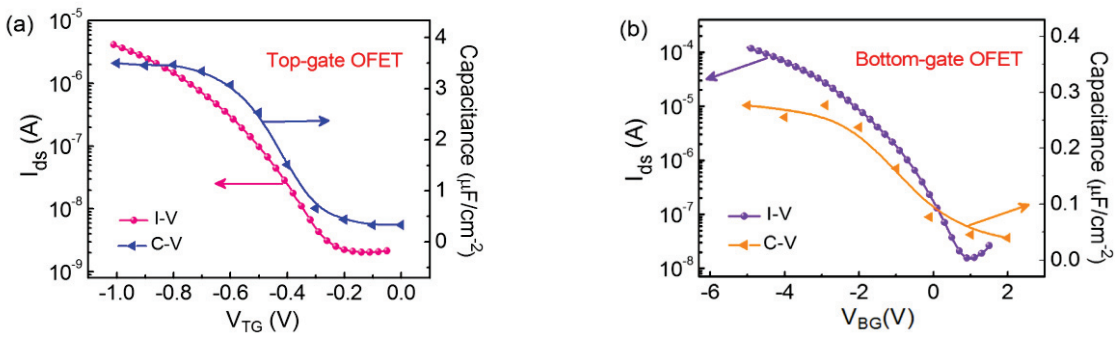

Figure 2. The transfer characteristics and effective capacitance-voltage (C-V) relations of (a) top-gate OFET and (b) bottom-gate OFET in the single-gate mode. The C-V characteristics were measured at 1 Hz.

To understand the effects of individual gates, we first operated the DG-OFET device in the "top-gate only" and "bottom-gate only" modes. Figure 2 shows the current-voltage (I-V) and effective capacitance-voltage (C-V) characteristics of the devices. (The effective capacitance values were extracted based on a parallel RC model.) Note that in the single-gate test mode, the connection of the other gate (floated or grounded) has little effect on the electrical characteristics of the devices. The effective areal capacitance densities of the bottom-gate dielectric and top-gate dielectric are measured to be around 0.3 μFcm^{-2} and 3.5 μFcm^{-2} respectively, suggesting a stronger field effect of the top-gate OFET. Based on the capacitance values, the extracted bottom and top FET mobilities are 0.15 $cm^2V^{-1}s^{-1}$ and 0.02 $cm^2V^{-1}s^{-1}$, respectively. There may be two reasons for such mobility difference. Firstly, the packing of the polymer chains at the bottom interface may be more ordered than that on the top interface; secondly, the saline solution may introduce trap states on the top interface, while the bottom interface is well passivated by the OTS layer. We note from previous studies that to achieve effective dual-gate operation, the top and bottom OFET channels should have comparable conductance, with mobility difference less than two orders.[5] Our DG-OFET device well fulfills this requirement.

We now examine the device behavior in the dual-gate mode. As shown in Figure 3a, the threshold voltage ($V_{th,TG}$) of the top-gate OFET can be gradually tuned towards positive when the bottom gate bias (V_{BG}) is varied from + 4 V to -3 V. Under a cell-friendly top-gate voltage of 0.2 V, the double-gated (V_{BG}=-3 V) channel current approaches ~10^{-7} A and the transconductance reaches 1.5 μS, three orders higher than that of the single-gated (V_{BG} floated). This tunability enables operation of the top-gate device at its most sensitive regime without damaging the biological species at the solid-liquid interface. The relationship between $V_{th,TG}$ and V_{BG} can be described with two linear fits, as presented in Figure 3b. The origin of the two linear relationships can be well explained by analyzing the working principles of the dual-gate devices. In a DG-OFET, both the top gate and bottom gate can induce a charge accumulation layer at their nearest semiconductor surface. If a negative bottom gate voltage V_{BG} is applied and exceeds the threshold voltage (in our devices the bottom-gate threshold voltage $V_{th,BG}$ is − 0.25 V), a bottom accumulation channel is formed. Accordingly, to turn the entire device to the OFF state, a more positive top gate bias (V_{TG}) is required, leading to a positive shift of $V_{th,TG}$. Such relation can be described with the following equation:[6]

$$\Delta V_{th,TG} = -\frac{C_{BG}}{C_{TG}} \Delta V_{BG} \qquad (1)$$

where C_{BG} and C_{TG} represent the capacitances of the top and bottom channel, respectively. According to the capacitance values extracted from the C-V measurements, the ratio of C_{BG} to C_{TG} is 0.0727, agreeing well with the fitted slope of 0.07598 in Figure 3b.

As V_{BG} moves towards positive, the bottom-gate OFET is switched from accumulation to depletion, and the depletion electric field gradually penetrates into the semiconductor bulk. As a result, the top gate-accumulated charge carriers are

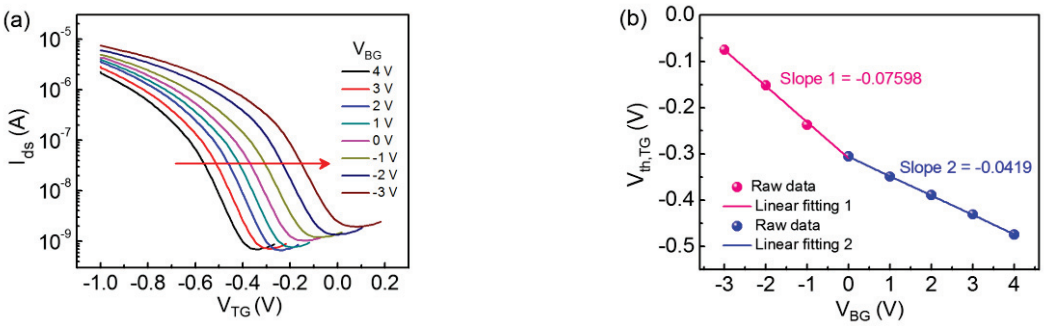

Figure 3. (a) Transfer characteristics of the top-gate OFET operated in the dual-gate mode with the bottom gate bias varying from +4 V to -3 V in steps of -1 V from left to right. The drain voltage was kept constant at -0.4 V; (b) Linear dependence of the top-gate OFET threshold voltage on the bottom gate bias (dots: data; lines: linear fitting).

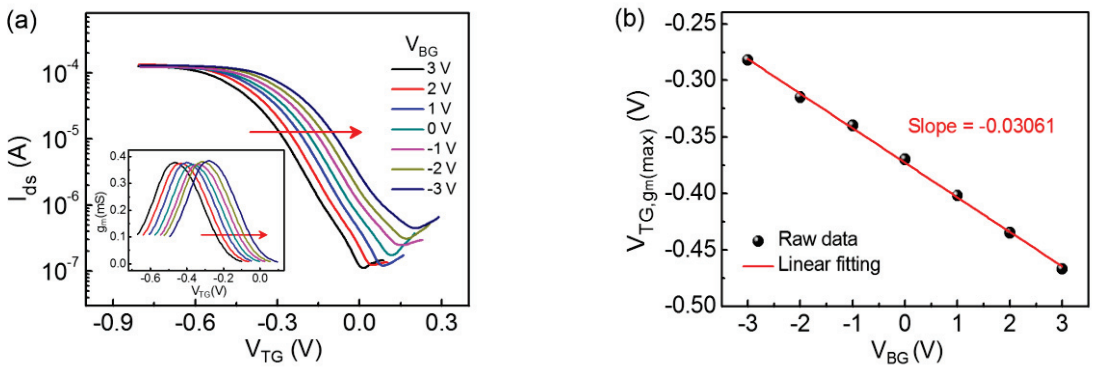

Figure 4. (a) Transfer curves of the top-gate OECT operated in the dual-gate mode with the bottom gate bias varying from +3 V to -3 V in steps of -1 V from left to right. The drain voltage is kept constant at -0.2 V. The inset figure shows the calculated transconductance corresponding to each transfer curve; (b) Linear dependence of the maximum transconductance voltage point on the bottom gate voltage. (dots: data; line: linear fitting)

depleted away by the bottom gate. The electrostatic coupling of the bottom-gate electric field and top-gate accumulation channel leads to a negative shift of $V_{th,TG}$ as described by the equations below: [7]

$$\Delta V_{th,TG} = -\frac{C_{BG}C_{OSC}}{C_{TG}(C_{BG}+C_{OSC}+C_{BG-it})}\Delta V_{BG} \quad (2)$$

$$\frac{1}{C_{OSC}} = \frac{1}{C_{TG,depletion}} - \frac{1}{C_{TG,accumulation}} \quad (3)$$

$$C_{BG-it} = D_{BG-it} \times Q \quad (4)$$

where C_{TG} and C_{BG} are the capacitances of the top and bottom channel, respectively; D_{BG-it} is the density of bottom interface states, C_{BG-it} is the corresponding interface capacitance, and C_{osc} is the depletion capacitance of the semiconductor. Here C_{TG}, C_{BG} and C_{osc} can be extracted from the C-V characteristics in Figure 2. Based on the fitted slope in the positive V_{BG} regime (blue line in Figure 3b), we calculate D_{BG-it} to be 1.4×10^{11} $cm^{-2}V^{-1}$, similar to those reported for other organic devices.

Finally, we examine whether the dual-gate effect can also be utilized to control the operation of OECTs. Here we investigate the g2T-T based DG-OECT structure shown in Figure 1b. This polymer has been previously shown to support p-type accumulation-mode OECT operation. Figure 4a illustrates the top-gate transfer curves of the OECT under different bottom gate voltages, and the inset plots the corresponding transconductance g_m. The result demonstrates again that with the additional gate, we are able to utilize the maximum device transconductance point within the cell-friendly voltage range. To quantitatively analyze the tuning of the maximum transconductance voltage point ($V_{TG,g_m(max)}$) by V_{BG}, we fit their relationship in Figure 4b. We note that, in this case, only one linear fit is required for all data points, which is different from the DG-OFET (Figure 3b). This is because in OECTs, ion doping and dedoping occur in the entire active layer. As a result, the bottom-gate and top-gate effects are always coupled. A similar behavior has been reported previously in dual-gate self-assembled monolayer field-effect transistor (SAMFET).[8] The relationship of $V_{TG,g_m(max)}$ and V_{BG} can thus be described by:

$$\Delta V_{TG,g_m(max)} = -\frac{C_{BG}}{C_{TG}}\Delta V_{BG} \quad (5)$$

The effective areal capacitance densities of the bottom-gate and top-gate dielectrics are measured to be 0.35 μFcm^{-2} and 11.2 μFcm^{-2}, respectively. The fitted slope of -0.03061 in Figure 4b agrees well with the ratio of C_{BG} to C_{TG} (0.03125), confirming the accuracy of the device model. We also performed the hMSC detachment sensing experiment using the g2T-T based OECT devices and found that the DG-OECT exhibits a larger current variation than the SG-OECT after cell detachment, which suggests that the dual-gate structure could improve the sensitivity of the OECT. However, the temporal response of the OECT sensing platforms is in general slower than that of the

OFET platforms, as the former involves a bulk ion diffusion process.

4. CONCLUSIONS

In summary, we have demonstrated a liquid-solid dual-gate organic transistor structure to enable cell sensing with maximum transconductance (i.e. maximum amplification). In our device design, the threshold voltage of the top liquid-gated conduction channel is controlled by a bottom gate that is separated from the semiconductor with an Al_2O_3/SiO_2 bilayer gate dielectric. With this design the threshold voltage of the "sensing channel" can be linearly tuned in a voltage window exceeding 0.4 V (from -0.475 V to -0.074 V). It is found that the voltage tuning at the negative bottom-gate bias is limited by redox reactions that could permanently break the oxide gate dielectric. Within the breakdown threshold, in general, the operation of the DG-OFET and DG-OECT devices can be well described with the device models developed for solid-state dual-gate transistors.

5. ACKNOWLEDGEMENT

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