A Novel a-IGZO TFT Scan Driver Circuit Using Only One Pull-Down Transistor

Jungwoo Lee[1], Jae-Hong Jeon[2], KeeChan Park[3], Soo-Yeon Lee[4] and Yong-Sang Kim[1]

yongsang@skku.edu

[1]Department of Electrical and Computer Engineering Sungkyunkwan University, Suwon, 16419, Korea
[2]School of Electronics and Information Engineering, Korea Aerospace University, Gyeonggi 10540, Korea
[3]Department of Electronics Engineering, Konkuk University, Seoul 05029, Korea
[4] Department of Electrical and Computer Engineering, Seoul National University, Seoul 08826, Korea
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ABSTRACT

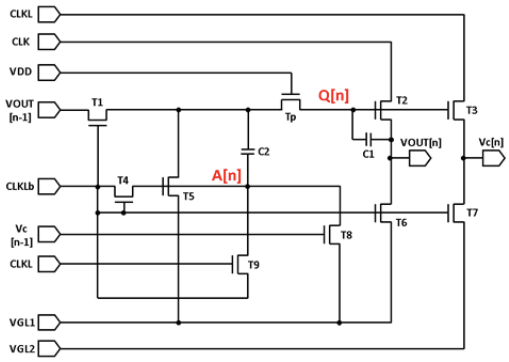
This paper proposes new scan driver to prevent output ripple voltage which can be generated by CLK. Using only one pull-down TFT with 50% turn-on duty ratio, proposed circuit can obtain both high reliability for continuous bias stress and fully cut-off ripple voltage by using negative VGS for pull-up TFT.

1 INTRODUCTION

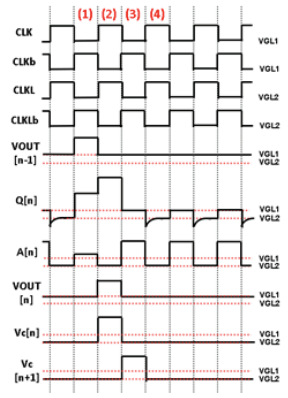
Recently, the oxide TFT has been noted for its higher mobility and low off-current compared to a-Si:H TFT. Nevertheless, there are two issues with oxide TFTs. The first issue is depletion mode operation with different indium component ratio. The oxide TFT can have negative threshold voltage (Vth) in initial state. In this case, TFT can be turned on even when the gate source voltage becomes zero bias condition [3]. Therefore, depletion mode operation can cause serious operation failures in the gate driver circuit such as output degradation and abnormal power consumption. The second issue is electrical characteristic variation due to the different bias stress. Continuous bias stress can cause electrical characteristics variation (on current reduction and Vth shift) due to charge injection or charge trapping between gate insulator and channel interface [4], [5].

Meanwhile, gate driver circuit is composed of input TFTs, pull-down TFTs, and pull-up TFTs which are responsible for stable voltage transfer to each pixel. In this case, the pull-down unit is always turned on to maintain the VOUT node at the low voltage except for output period. Therefore, the pull-down TFT should be driven by DC-type. However, DC-driven method can result in electrical deterioration of the TFT since continuous bias stress is applied to the TFTs. To prevent this phenomenon, many groups proposed the gate driver circuit structures to ensure the high electrical stability [6], [7]. As one of the methods to ensure stability, AC-driven method for the pull-down unit is proposed [7]. However, conventional AC-driven method can increase the circuit complexity since two or more pull-down TFT structures are needed.

To overcome these problems, we propose a simple a-IGZO TFT scan driver circuit ensuring the reliability of the pull-down TFT. Although the proposed circuit is composed of only one pull-down TFT with a 50% duty ratio, the output stage can be discharged at a 100% duty ratio to maintain the stability. Also, the reliability of the pull-down TFT against bias stress can be reduced by adjustment of turn-on duration . In addition, the leakage path due to the pull-up TFT is completely blocked to prevent the ripple voltage. And, it operates stably in both the depletion mode and the enhancement mode.



(a)



(b)

Fig. 1. Proposed scan driver circuit (a) schematic (b) Timing Diagram

2 Proposed Gate Driver Circuit

Fig. 1 (a) and (b) show the proposed scan driver circuit schematic and timing diagram. The proposed circuit consists of ten TFTs and two capacitors. The circuit has four clock signals which are the two pairs of two-phase clocks with different low levels. CLK voltage swings from -5 V to + 28 V and CLKL voltage swings from -13 V to + 28 V. Also, VGL1 and VGL2 signals, which are DC-type voltage supply, are -5 V and -13 V, respectively. The operation of the proposed circuit can be divided into four sections.

2.1 Pre-charging

As CLKLb and VOUT[n-1] become VGH, Q[n] voltage is charged up to VGH-V_{TH_T1} through T1. Therefore, VOUT[n] is discharged through T2 and T6 to maintain the VGL voltage, and T5 is turned off because the A[n] voltage is discharged through T8.

2.2 Bootstrapping

When CLKLb becomes VGL2, the Q[n] becomes floating state. At this time, as CLKL and CLK become VGH, Q[n] is bootstrapped using C1. Thus, the driving capability of the pull-up TFTs T2 and T3 is improved to transmit the output voltage to VOUT[n] and Vc[n]. In addition, if the Q[n] node voltage rises twice as high as the VGH, it cannot be transferred to the drain node of T1 because Tp is turned off in this period. Therefore, stability of both the output node and the input TFT can be ensured.

2.3 Reset & Low holding 1

Since CLKLb becomes VGH again, VGH-V_{TH_T4} is stored in A[n] through T4. Accordingly, the Q[n] voltage is discharged through T5, and VOUT[n] and Vc[n] are discharged with a 50% duty ratio through T6 and T7, respectively. In this section, Q[n], the upper part of C2, is discharged to VGL1, and A[n], the lower part of C2, is charged with VGH-V_{TH_T4}, so the VGH-V_{TH_T4}-VGL1, which is the voltage difference between both ends of the capacitor, is stored in C2.

2.4 Low holding 2

As CLKLb becomes VGL2 and CLKL becomes VGH, the voltage of A[n] is discharged to VGL2 of CLKLb through T9. Therefore, since Q[n] becomes floating, it drops to a lower voltage than VGL1 due to the coupling effect by C2. As a result, since the gate-source voltage of T2 has a negative value, the T2 is completely turned off to block ripple voltage which can be generated by CLK variation. Also, in this section, VOUT[n] is discharged with a 50% duty ratio through T1 and T5 of the stage[n+1] because A[n+1] voltage is charged up to VGH-V_{TH_T4}. The proposed circuit maintains the VGL voltage stably in the off-stage while repeating section 3 and 4 after the output period.

3 Results and Discussion

Table 1 shows the design parameters of the proposed gate driver circuit. The frame frequency is 60 Hz and 1 line time is 7.6 μs based on Ultra High Definition (UHD) resolution display panel (3840×2160). All the channel length of TFTs is 5 μm, and the channel width of the pull-up TFT is 850 μm. We used SmartSpice program to verify the capability of the proposed circuit. Fig. 2 shows the simulated I-V transfer characteristics of the a-IGZO TFT used in the proposed circuit. The channel width and length are 180 μm and 5 μm, respectively, which is the same parameters based on the pull-down TFT. The V_{TH} is set to +2.0 V and mobility is 4.3 $cm^2/V{\cdot}s$. Fig. 3 shows the simulated voltage waveforms of A [n], Q [n] and VOUT [n] node when the proposed circuit operates in depletion mode and enhancement mode operation. We applied a 3 kΩ resistor and a 220 pF capacitor to every VOUT node to emulate the gate line load. In the Fig. 3 (a), the threshold voltage of all TFTs is shifted to -4.0 V, which is the negative Vth margin. The Q [n] node is pre-charged to +28 V and bootstrapped to almost +52 V without any voltage loss. Thus, the output is generated at the VOUT node stably with +28 V. The A [n] node voltage is also maintained at +28 V stably with a 50% duty ratio which means that the voltage difference (VGH-Vth_T4-VGL1) is stored in C2 assuredly.

Table 1. Design parameters of the proposed gate driver

Proposed circuit			
L	5 μm	C1	0.3 pF
T1 W	100 μm	C2	0.6 pF
T2 W	850 μm	CLK voltage	-5 V ~ +28 V
T4 W	40 μm	CLKL voltage	-13 V ~ +28 V
T5 W	50 μm	VGL1	-5 V
T6, T7 W	180 μm	VGL2	-13 V
T8 W	160 μm	CLK frequency	65.8 kHz
L = TFT length, W = TFT width			

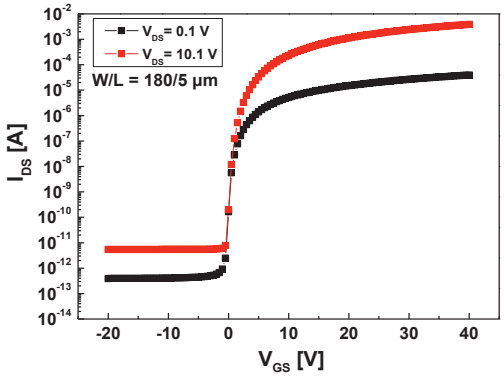
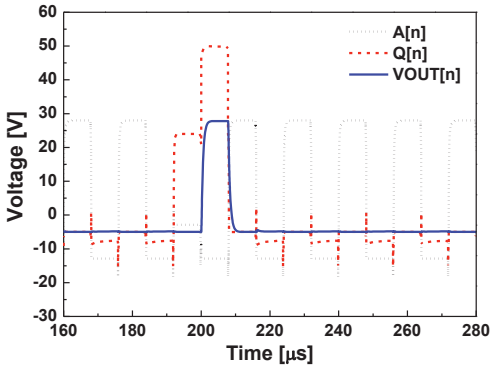
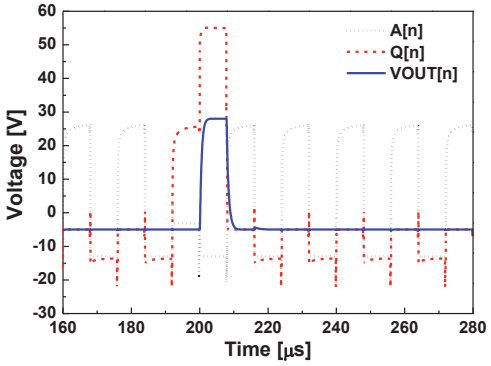


Fig. 2. I-V characteristics of a-IGZO TFT



(a)



(b)

Fig. 3. Simulated voltage waveforms of A[n], Q[n] and VOUT[n] node (a) V_{TH} = -4.0 V (b) V_{TH} = +2.0 V

Therefore, the Q node is boosted down to -8.9 V in the next period to turn off the pull-up TFT completely with 50% duty ratio. In the Fig. 3 (b), The threshold voltage of all TFTs is shifted to +2.0 V. Q[n] is pre-charged to +26 V excluding the threshold voltage of T1, then bootstrapped to +55.1 V. Thus, a complete VGH of +28 V is transmitted to VOUT[n]. In addition, as the +26.0V voltage charged in A[n] is discharged to -13.0 V, the Q[n] voltage drops from -5 V to almost -15.0 V. Therefore, the gate-source voltage of the pull-up TFT becomes about -10.0 V which means that the leakage path is completely blocked. In the Fig. 5 (a), The output of the VOUT node maintains a peak voltage of +28V regardless of the V_{TH} shift. According to Table 2, when the V_{TH} of the entire TFT is 0V, the rising time and falling time of the output waveform are 1.06 μs and 1.29 μs, respectively. Also, when the V_{TH} shifted to +10V, rising time and falling time are 1.99 μs and 1.85 μs, respectively. Therefore, it can be confirmed that the proposed circuit operates stably despite the V_{TH} shift.

4 CONCLUSIONS

we proposed a new a-IGZO TFT scan driver circuit which use a single pull-down TFT. The proposed circuit was discharged at a duty ratio of 50% through the pull-down TFT of stage [n] and the remaining 50% duty ratio was discharged through the pull-down TFT of stage [n+1]. Therefore, even if one pull-down TFT is used, reliability of the pull-down TFT and the VOUT[n] was ensured simultaneously because the VOUT[n] was discharged with a total 100% duty ratio. In addition, since the pull-up TFT was completely turned off by the coupling effect, ripple voltage could be prevented, and it operated stably in both the depletion mode and the enhancement mode. According to the simulation results, when the threshold voltage of the entire TFT is -4.0 V and +2.0 V, the output voltage of +28.0 V is transmitted stably without any voltage loss. Also, when the Q[n] is boosted down to -15 V, the ripple voltage of VOUT [n] was within 2.4% of the total swing voltage.

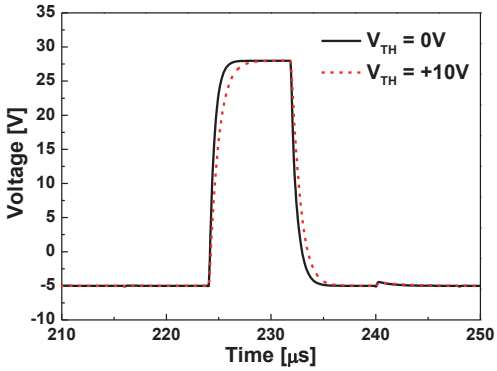


Fig. 4. The simulated VOUT [n] voltage waveforms at V_{TH} = 0 V and V_{TH} = +10.0 V

Table 2. Output characteristic of the proposed circuit

V_{TH} of all TFTs	Rising Time [μs]	Falling Time [μs]
0 V	1.06	1.29
+10 V	1.99	1.85

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