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Organic Floating-Gate Transistors with Hole Trapping Characteristics for NAND-Like Memory Operation

Miho Higashinakaya[*], Takashi Nagase[*,], Reitaro Hattori[*], Shion Tazuhara[*], Takashi Kobayashi[*,**], Hiroyoshi Naito[*,**]**

* Department of Physics and Electronics, Osaka Prefecture University, Sakai 599-8531, Japan
** The Research Institute for Molecular Electronic Devices (RIMED), Osaka Prefecture University, Sakai 599-8531, Japan

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ABSTRACT

Solution-processable organic floating-gate transistor memories programmable in the dark have been developed using ambipolar polymer semiconductor. Solution-processed organic transistor memories allow the storage of holes as well as electrons by tuning the work function of gate electrodes. We demonstrate NAND-like memory operation using organic transistor memories with hole trapping characteristics.

1. INTRODUCTION

In recent years, nonvolatile organic memories using organic field-effect transistors (OFETs) have attracted growing interest as data storage media for flexible and printed electronic devices because they allow fabricating memory circuits by similar processes used for organic integrated circuits. As OFET technology moves close to practical use, it is highly desirable to fabricate floating-gate OFET memory devices and organic memory circuits by coating and printing techniques. However, the fabrication of floating-gate OFET memories by solution processes remains difficult because it generally requires the preparation of multiple organic layers without interfacial mixing. To realize the solution processing of floating-gate OFET memories, we have adopted top-gate OFETs with polymer semiconductor layers, which enables to deposit organic charge storage layers onto the organic semiconductor layer because of the availability of various orthogonal solvents for polymer semiconductors. We have shown that poly(3-hexylthiophene)-based OFET memories with polymer/small-molecule composite charge storage layers exhibit excellent memory operations by programming under light illumination [1].

In this paper, we report on solution-processable OFET memories programmable in the dark. The developed OFET memories exhibit ambipolar trapping behavior and the type of trapping carriers can be controlled by tuning the work function of gate electrodes. We show that the use of OFET memories with hole trapping characteristics allows the memory operation in connected memory devices in series, *i.e.,* NAND flash memory. Such configuration is attractive for reducing the number of metallic wires in OFET memory circuits; however, only a few studies have been reported [2].

2. EXPERIMENTS

Fig. 1 shows the schematic illustration of the top-gate OFET memory device and the memory array used in this study. To fabricate a OFET memory programmable in the dark, we used an ambipolar polymer semiconductor, poly(*N*-alkyldiketopyrrolo-pyrrole-dithienylthieno[3,2-b] thiophene) (DPP-DTT), which was spin-coated using chloroform on glass substrates having Au source-drain electrodes. An organic composite of polystyrene (PS) and 6,13-bis(triisopropylsilylenthynyl) pentacene (TIPS-PEN) (a weight ratio of 80:20) was spin-coated on the DPP-DTT layer using its orthogonal solvent (*n*-butyl acetate) to fabricate the organic floating-gate layer on the organic semiconductor layer. After CYTOP or CYTOP/parylene was deposited on the PS:TIPS-PEN layer, Al or MoO_3/Al gate electrodes were evaporated on top of the CYTOP or CYTOP/parylene layers to investigate the effect of the work function of gate electrodes on memory characteristics. Finally, the memory devices on the substrate were isolated by removing organic layers by O_2 plasma etching using the gate electrodes as the etching mask.

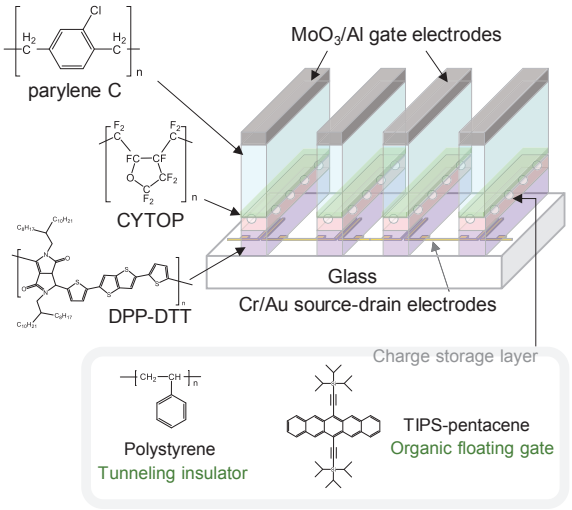

Fig. 1 Structure of a solution-processed top-gate OFET memory array based on the ambipolar polymer semiconductor of DPP-DTT.

3. RESULTS AND DISCUSSION

Figures 2(a) and (b) show the transfer characteristics of DPP-DTT FET memory devices with Al and MoO_3/Al gate electrodes before and after programming and erasing, respectively. Both devices exhibit large positive threshold voltage (V_{th}) shifts from the erased state when the positive gate voltage (V_G) of +60 V is applied in the dark. The positive V_{th} shifts are attributed to the storage of electrons in organic floating gates composed of TIPS-PEN molecules. Since DPP-DTT has the deep lowest unoccupied molecular orbital (LUMO) (−3.5 eV) and a good electron transport property, electrons can be injected from Au source electrodes and transferred to the LUMO level of TIPS-PEN floating gates (−3.55 eV) through the DPP-DTT semiconductor layer, as shown in Fig. 3(a).

It can be seen in Fig. 2(b) that the DPP-DTT FET memory with the MoO_3/Al gate electrode shows a larger

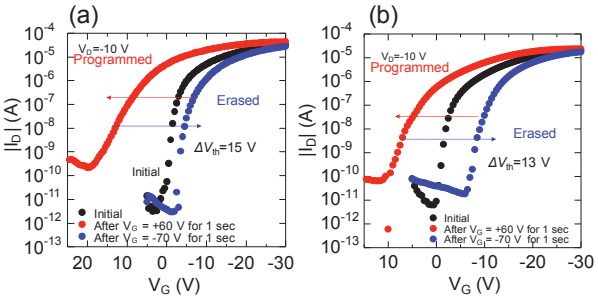

Fig. 2 Transfer curves of DPP-DTT FET memory devices with (a) Al and (b) MoO_3/Al gate electrodes measured before and after programming (V_G = +60 V, 1 s) and erasing (V_G = −70 V, 1 s) in the dark.

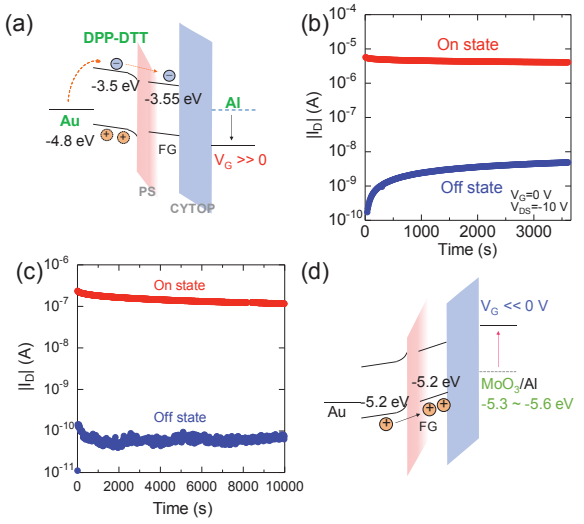

Fig. 3 (a) Energy band diagram of the DPP-DTT FET memory with the Al gate electrode. Retention characteristics of DPP-DTT FET memories with (b) Al and (c) MoO_3/Al gate electrodes. (d) Injection of holes into TIPS-PEN floating gates in the memory with the MoO_3/Al gate electrode.

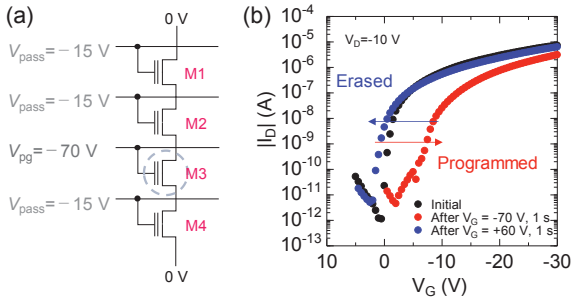

Fig. 4 (a) Programming process of a 1×4 memory array. (b) Programming and erasing characteristics of the M3 device obtained from the connected DPP-DTT FET memory array.

negative V_{th} shift under application of the negative V_G of −70 V, indicating that holes are injected and stored in the TIPS-PEN floating gates. We also see from Figs. 3(b) and 3(c) that the device with the MoO_3/Al gate electrode exhibit the good retention characteristics of the drain current (I_D) in the off state measured at V_G = 0 V. As the MoO_3 films have a high work function (−5.3 to 5.6 eV), the injection of electrons from the Au source electrode to the TIPS-PEN floating gates can be inhibited during the readout with V_G = 0 V. Instead, the injection of holes can be enhanced in the device with the MoO_3/Al gate electrode under application of the negative V_G, as shown in Fig. 3(d).

Using the memory devices with hole storage characteristics, NAND-like memory operations can be obtained in the 1×4 memory array composed of memory devices connected in series [Fig. 4(a)]. As shown in Fig. 4(b), the memory device M3 shows negative V_{th} shifts by programming at V_G = −70 V when the devices M1 and M2 are operated as the p-type transistor at V_G = −15 V. The results demonstrate that holes injected from the source electrode were conducted through the devices M1 and M2 and trapped in the device M3. Such NAND-like operation has not been reported in floating-gate OFET memories because most existing floating-gate OFET memories exhibit memory characteristics by storing of minority charge carriers [3].

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