High Reliable Integrated Gate Driver GOA Circuit using Four-Mask a-Si TFT for Large Size UHD LCD TVs

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Key words: GOA, Four-mask process, Model Card, process fluctuation, TFT reliability

Abstract

Gate driving circuit (GOA) design is critical to reduce the production cost and narrow border TFT-LCD. The proposed GOA circuit has the optimized TFT W/L design and TFT stress reduction which enhances gate driver reliability for TV application. We developed 50UHD 120Hz TFT-LCD with GOA circuit using 4-mask a-Si TFT.

1. Introduction

TFT-LCD is widely used in display, where gate driver on array (GOA) is the current mainstream with the advantages of low cost and narrow border [1-3]. GOA is based on the control signal provided by the external circuit (CLK, Input and VDD signal). Amorphous silicon (a-Si) TFT technology is suitable for large area applications because of its low cost, low temperature processing and better uniformity. LCDs display using a-Si:H TFT technology as backplane is still the major product in large size display field. However, instability of a-Si is the major factor that hinders stable circuit operation using a-Si TFT. A-Si has meta-stability which is regarded as thermal equilibration process including elements such as band-tail carriers, Hydrogen, weak bonds and dangling bonds, whether it is about defect creation or charge trapping [4-6]. Degradation of a-Si TFT is inevitable when it is deviated from as deposited equilibrium by the applied bias voltage. Usually bias stressed a-Si TFT shows increase in threshold voltage with time. Circuits using a-Si TFT also show degradation of the circuit characteristics because of the degradation of constituent TFTs. In addition, the mobility of a-Si:H TFT is about 0.2-0.4 cm2/V-s, which is less than oxide-TFT and poly-Si. It indicated that the size of the a-Si TFT should be much large to drive the gate line loading. Therefore, the number of TFT in the GOA unit is need to be control at the minimal value and the parameters should be optimized for gate driver circuit design.

It exist process fluctuation problem in the manufacture of TFT and GOA driver circuit for TFT-LCD. We should know poor TFT performance which is due to the process fluctuation whether can also satisfy GOA circuit. It is important to predict the each W/L size TFT properties because that there are many kinds of different W/L size. The main purpose of this work is to find circuit margin by estimating different W/L TFT size performance. In this paper, we present the high reliable integrated gate driver GOA circuit using 4-mask a-Si TFT for large size and high resolution TFT-LCD TVs application.

2. Results

2.1 Driving of GOA Circuit

Fig.1 shows the schematic diagram of proposed GOA driving circuit. This circuit contains some TFTs with small width over channel length (W/L). As channel length (L) has little impact on device stability, W/L can amplify with same ratio to improve the process uniformity. Duty ratio of GOA clock signal (CLK) could be modified to improve the TFT stability after long time operation and guarantee our GOA circuit performance.

In the GOA driver circuit, TFT plays important role. TFT performance may change due to fluctuations in the production process should also be reflected in the simulation.

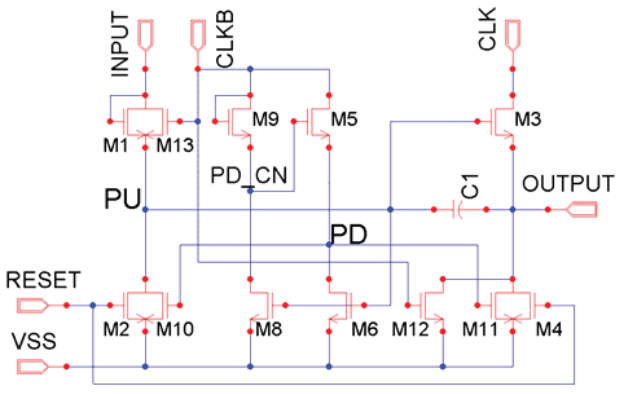

Fig.1 The schematic diagram of proposed GOA driving circuit.

2.2 TFT Ratio of GOA Circuit

The ratio of TFT with different functions is obtained by TFT model card and GOA circuit simulation with the optimization of VGH, CKL, VSS. Step1: GOA circuit 1st Simulation is based on TFT corner Model Cards. Corner modeling are considered the array process

fluctuation and margin (Fig. 2). Step2: GOA circuit 2nd simulation is based on reliability stress Model Cards. Reliability stress Model Cards are considered the situation of TFT Ion decreasing and Vth shift (Fig.3). In Fig.4 shows the schematic diagram of proposed GOA driving circuit (T6~T11). The Vth shift margin is related to the voltage setting of P-node. The higher the voltage setting at P-node, the greater the margin of Vth shift. The voltage setting of P-node is related to the ratio of T11/T6 and T10/T7. Under the same TFT characteristics, the lower the ratio of T11/T6 and T10/T7, the higher the potential of P-node, the better the holding ability of Gate-off, and the greater the Vth shift margin. In Fig.5 shows the schematic diagram of proposed GOA driving circuit (T1~T5). We study the TFT reliability after 50C, 500 hours HTO (high temperature operation) RA stress (Fig.6).

2.3 Leakage Current

As shown in Fig.7, smaller channel length easy to get worse GOA reliability phenomenon. The leakage current of TFT is positively correlated with the Width/Length ratio of channel with process fluctuation. In this paper, it is very dependent on the stability of TFT characteristic. Under the condition of fixed working voltage (VGL and VGH), the drift of TFT transfer curve (up and/or right) will increase the leakage current.

2.4 Gate Driver Integrated GOA Panel Fabrication

Fig.8 shows the display images of the 50 inch UHD 120Hz TFT-LCD panel with the proposed integrated gate driver GOA circuit using 4-mask a-Si TFT which was fabricated on HKC display's G8.6 (H2) LCD line. Specifications of the gate driver integrated GOA panel are summarized in Table 1

3. Conclusions

GOA has been the mainstream of line addressing design in display. The design methodology for gate driving circuit (GOA) is critical to reduce the production cost and power consumption for TFT-LCD. The process fluctuation in the manufacturing of TFT can cause the malfunction of GOA. The proposed gate driver has single-scan control circuit with optimized TFT W/L design and TFT stress reduction circuit which enhances gate driver reliability for TV application. We evaluate the life time of the gate driver GOA in the accelerated condition. The stability of GOA is easily affected by the ratio of TFT with functions and the characteristics of TFT (leakage current). We successfully developed 50-inch UHD 120Hz TFT-LCD panel with the integrated gate driver GOA circuit using 4-mask a-Si TFT.

Acknowledgements

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4. References

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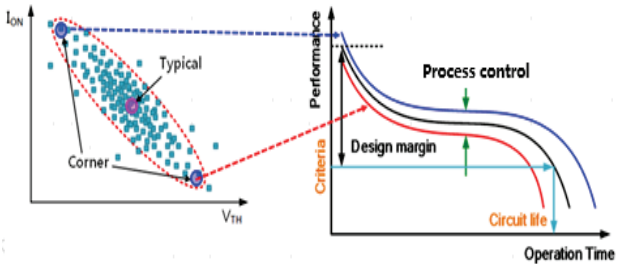


Fig.2 GOA circuit 1st simulation using the TFT corner Model Cards

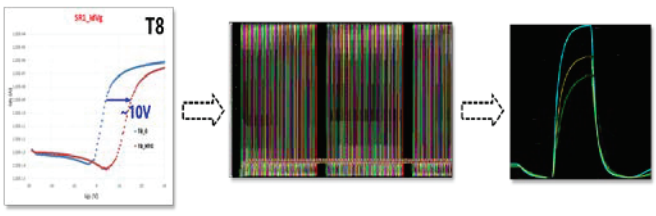


Fig.3 GOA circuit 2nd simulation using the reliability stress Model Cards.

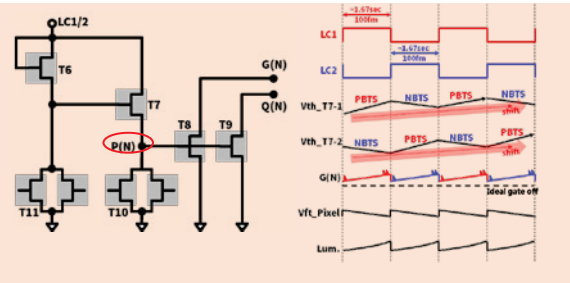


Fig.4 The schematic diagram of proposed GOA driving circuit (T6~T11)

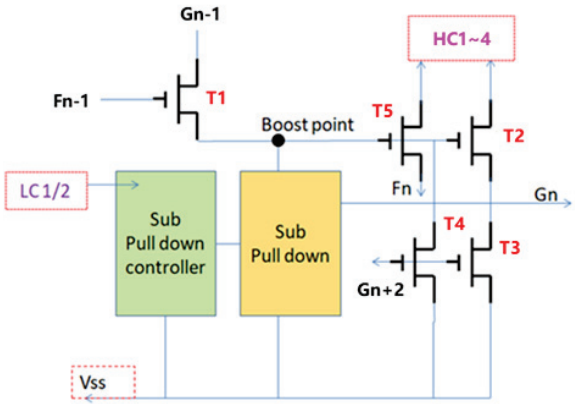
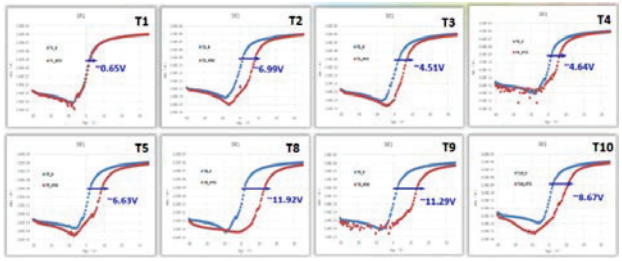


Fig.5 The schematic diagram of proposed GOA driving circuit (T1~T5)



Vth Shift margin	TFT device
10V~12V	T8、T9
8V~10V	T10
6V~8V	T2、T5
4V~6V	T3、T4
<4V	T1

Fig.6 TFT reliability measurement after 50C, 500 hours HTO RA stress

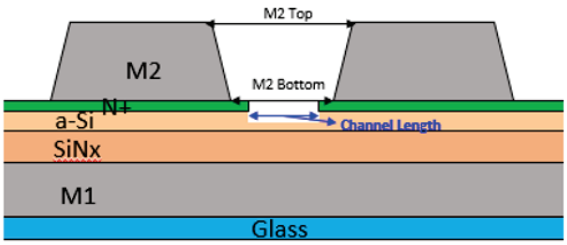


Fig.7 a-Si array structure with TFT channel architecture

Fig.8 50 inch UHD 120Hz TFT-LCD panel with the proposed integrated gate driver GOA circuit using 4-mask a-Si TFT

Table 1. Specifications of the gate driver integrated GOA panel

Item	Content	Unit
Panel size	50	inch
Resolution	3840(H)×2160(V)	_
Frame rate	120	Hz
Contrast ratio	5000:1	_
Array Structure	1G1D	_
No. of GD-IC	0	_
No. of SD-IC	12	_