Key Requirements for Manufacturing Micro LED Displays

Khaled Ahmed

khaled.ahmed@intel.com

Intel Corporation, 2200 Mission College Blvd, Santa Clara, California 95123, USA

Keywords: Micro LED, Display, Low Power

ABSTRACT

Manufacturing cost is the highest risk for μ LED displays. μ LED display cost is composed of backplane and frontplane costs. Backplane cost may be similar to OLED displays. The major cost contributors for frontplane are epitaxy, transfer, and defect management. Here, the technology requirements for manufacturing high performance, cost-effective μ LED displays are discussed.

1 INTRODUCTION

Micro LEDs (µLEDs) are being explored to make direct-view flat-panel displays [1-5]. Direct-view displays, used in automotive, smartphones, tablets, mobile PCs, monitors, and TVs, among other applications, represent most of the revenue in the display market. The ability to accurately and reliably transfer or otherwise integrate millions of µLEDs and electrically connect them to the driving circuitry (e.g. made of TFTs) is critical for commercial success. In particular, if LED manufacturing techniques could be used to produce billions of µLEDs on a single 300mm silicon wafer, and if such devices could be efficiently and accurately transferred to large substrates and connected to an active matrix, µLED displays could be cost competitive with existing LCD and OLED technologies. A key challenge is the need to distribute the µLEDs over a much larger area than the wafer on which they were grown.

For μ LED displays to be successful against incumbent display technologies, they must provide: (1) low power consumption, (2) high display quality, and (3) acceptable cost.

2 LOW POWER CONSUMPTION

In μ LED displays a desired color and luminance value are created from various combinations of three colors of light emitting elements (red, green and blue). Given that these differently colored light-emitting elements can have dramatically different efficacies, power consumption can be significantly influenced by the proportions of light produced by each of these elements. One way to compare different displays is compare their efficiency to produce white color. The required μ LED external quantum efficiency to achieve a desired power reduction with respect to OLED is shown in Fig. 1.

The display size is ~5.8" and resolution is ~QHD.



Fig. 1. Simulated external quantum efficiency (EQE) contours for μ LEDs to achieve display emitter power consumptions of 671mW (blue curve) and 671/3 mW (green curve), respectively. All white (D65) condition is assumed. The blue EQE was fixed at 10%. The labels represent power reductions. The 671mW value represents the power consumption of a commercial smartphone display with OLED technology [6].

3 HIGH DISPLAY QUALITY

µLED display pixels are composed of red, green, and blue sub-pixels. The output of each sub-pixel is individually controlled. Luminous flux and color are determined at the pixel level by combining the subpixel outputs. Due to production discrepancies, there may be variations in luminous flux for the same electrical signal input throughout the population of same-colored (same emission peak wavelength) sub-pixels on the display. This results in differences in color accuracy from pixel to pixel. In such a case, the result may be line "mura", which appears as a well-defined horizontal and/or vertical line across the µLED display. Line "mura" can also result from µLEDs with the same external quantum efficiency but with variance in emission peak wavelengths of red, green, and blue µLEDs. This may be avoided by using very uniform epitaxial growth process and equipment. A Monte Carlo analysis along with physics-based color mixing models have been used to estimate targets for the variance of color peak wavelengths for red, green, and blue µLEDs in order to meet color uniformity targets as specified by the display application. This is shown in Fig. 2. The estimated targets were compared with experimental data reported by multiple industrial companies [7-10]. The mathematical framework and calculation algorithm were also used to estimate the required variance of μ LEDs' external quantum efficiency on a single wafer and from wafer-to-wafer in order to meet the color uniformity desired for high quality displays. This is shown in Fig. 3.



Fig. 2. Estimated target standard deviation of peak wavelengths for red, green, and blue colors for various White color points along the Planckian locus. D65 white has a color temperature of 6500K.



Fig. 3. Estimated range of variation of D65 white color CIE indices (u and v) as function of standard variation of EQE (as a percentage of mean EQE). The peak wavelengths for red, green and blue colors were 630nm, 532nm, and 467nm, respectively. Solid line is Δu and dotted line is Δv .

4 DISPLAY PRODUCTION COST

4.1 Wafer Size

The number of displays that can be manufactured from a single wafer depends on the specifics of the transfer technology, size of the wafer, the μ LED pitch on the wafer, and the resolution and size of the

display. Fig. 4 shows the number of MOCVD tools per 10 million displays as a function of display size when the wafer size is 6", 8" or 12" in diameter. The MOCVD epi process needed to make the μ LED structure is assumed to be ~3 hours/wafer. Larger wafer diameter results in more practical demand for the number of MOCVD epi tools.



Fig. 4. Simulated number of MOCVD epi tools as a function of display size. The MOCVD throughput is fixed at 3 hours/wafer, and the μ LED size was fixed at 4 μ m. The wafer diameter is shown on each curve. The stamp size is 1".

4.2 Micro LED Transfer Throughput

The throughput of micro transfer depends on the transfer technology details. The transfer throughput for two technologies are compared in Fig. 5 as function of display size. A truly massive transfer technology is desired for cost-effective large displays.



Fig. 5. Simulated transfer throughput versus display diagonal for (1) pick & place and (2) truly massive transfer methods.

4.3 Micro LED Size

The estimated average selling price for a smartphone display of size 6" in diagonal is plotted versus μ LED size in Fig. 6. As the μ LED size

decreases, the ASP decreases. For a given μ LED size, scaling the wafer size from 8" to 12" diameter results in significant reduction of ASP.



Fig. 6. Simulated 6" display/QHD average selling price versus μ LED size for two different wafer sizes (8" and 12" diameter). The stamp size is 1". The wafer size and μ LED size have significant impact on the display ASP.

4.4 Yield and Redundancy

In μ LED displays a fault means that a μ LED does not emit light due to defects during the semiconductor process steps of making the μ LEDs on the donor wafers, or due to poor or no bonding to the display backplane when the μ LEDs are transferred from the donor wafer to the display backplane. A display failure means that the display has more than a specified maximum number of faulty (e.g. dark) pixels. This number is many cases is zero. Recently, the author developed a yield model for a μ LED display. The model accounts for redundant subpixels (μ LEDs) per color per pixel. The model is described by the equations [11]:

$$p = y_t \times y_w \tag{1}$$

$$q = 1 - p \tag{2}$$

$$p_p = 1 - \left(\sum_{k=0}^{R-1} \binom{R}{k} q^k (1-q)^{R-k}\right)^3$$
(3)

$$Y = \sum_{i=0}^{m} {N \choose i} p_p^i (1 - p_p)^{N-i}$$
(4)

The term y_t represents transfer yield, and y_w represents wafer die yield. *R* represents the redundancy level (i.e. the number of µLEDs per color per pixel). *Y* is the display line yield. *m* is the maximum number of acceptable defective pixels on a display. Ideally, this value should be zero. Contours of the required wafer die yield and transfer yield for a display line yield of 50% are shown in Fig. 7. The display has a resolution of QHD.



Fig. 7. Simulated wafer die yield versus transfer yield for a display line yield of 50%, resolution of 2550x1440, and redundancy of 1.

When redundancy is used, the required wafer and transfer yields become more practical and achievable as shown in Fig. 8 and Fig. 9.



Fig. 8. Simulated wafer die yield versus transfer yield for a display line yield of 80%, resolution of 2550×1440.



Fig. 9. Calculated defect density for wafer and transfer process required to achieve a display line yield of 80% with various redundancy values (R = 1-5).

4.5 Repair

During the manufacturing of a μ LED device, a defective μ LED may be found on a receiving substrate after μ LEDs are transferred to the receiving substrate. In this situation, a repair for the defect is required, which is called a μ LED repair or repairing a μ LED. Test and repair of μ LED displays including micro devices transferred to the system substrate is very crucial to increase the yield. The enabling of easy and/or practical repair processes to increase the yield and reduce the cost is highly desired. The number of defective μ LEDs on a display with total number of pixels = N, and redundancy of R can be estimated by the following model equation:

$$N_{d} = \sum_{i=0}^{R} \sum_{j=0}^{R} \sum_{k=0}^{R} N(i+j) + k) \left(\binom{R}{i} q^{i} (1) - q)^{R-i} \binom{R}{j} q^{j} (1) - q)^{R-i} \binom{R}{k} q^{k} (1-q)^{R-k} \right)$$
(5)

where *p* is given by (1) and *q* is given by (2), and R is the redundancy level (R = 1 means no redundancy). The calculated number of defective μ LEDs on a display is shown in Fig. 10 as a function of transfer and die yield. Displays with different resolutions were assumed. The number of defective μ LEDs increases by ~100x as the transfer and die yields decrease from 99.99999% to 99.999%.



Fig. 10. Calculated number of defective µLEDs as a function of wafer die yield and transfer yield for three different resolutions. No redundancy is used.

5 CONCLUSIONS

Manufacturing cost is the highest risk for μ LED displays. The major cost contributors for μ LED displays are epitaxy, transfer, and defect

management. The requirements related to these aspects were analyzed quantitatively, and key numerical requirements were presented.

REFERENCES

- [1] N. Sugiura, C.-T. Chuang, C.-T. Hsieh, C.-T. Wu, C.-Y. Tsai, C.-H. Lin, C.-C. Liu, C.-Y. Liu, C.-N. Yeh, C.-Y. Liu, and Y.-C. Lin, "12.1-inch 169-ppi Full-Color Micro-LED Display using LTPS-TFT Backplane," *SID Symposium Digest* of *Technical Papers*, pp. 450-453 (2019).
- [2] G. Biwa, M. Doi, A. Yasuda, H. Kadota, "Technologies for the Crystal LED Display System," *SID Symposium Digest of Technical Papers*, pp. 121-124 (2019).
- [3] R. Chaji, E. Fathi, and A. Zamani, "Essentials of MicroLED Display Production," *SID Symposium Digest of Technical Papers*, pp. 323-327 (2020).
- [4] V. R. Marinov, "Laser-Enabled Extremely-High Rate Technology for µLED Assembly," *SID Symposium Digest of Technical Papers*, pp. 692-695 (2018).
- [5] M. Meitl, E. Radauscher, S. Bonafede, D. Gomez, T. Moore, C. Prevatte, B. Raymond, B. Fisher, K. Ghosal, A. Fecioru, A. J. Trindade, D. Kneeburg, and C. A. Bower, "Passive Matrix Displays with Transfer-Printed Microscale Inorganic LEDs," *SID Symposium Digest of Technical Papers*, pp. 743-746 (2016).
- [6] K. Ahmed, "Micro LEDs Efficiency Targets for Displays," *SID Symposium Digest of Technical Papers*, pp. 125-128 (2019).
- [7] A. Beckers, D. Fahle, C. Mauder, T. Kruecken, A. R. Boyd, M. Heuken, "Enabling the Next Era of Display Technologies by Micro LED MOCVD Processing," *SID Symposium Digest of Technical Papers*, pp. 601-603 (2018).
- [8] A. R. Boyd, A. Beckers, M. Eickelkamp, A. Alam, M. Heuken, "Enabling MOCVD Technology for Micro LED High Volume Manufacturing," *SID Symposium Digest of Technical Papers*, pp. 342-345 (2019).
- [9] P. Gilet, I.-C. Robin, "Nanostructures on Silicon to Solve the Active Display Paradigms," *SID Symposium Digest of Technical Papers*, pp. 684-687 (2018).
- [10] A. Paranjpe, J. Montgomery, S. M. Lee, "Manufacturing Solutions for Micro-LED Displays," *SID Symposium Digest of Technical Papers*, pp. 169-172 (2019).
- [11] K. Ahmed, "Yield Statistics for Fault-Tolerant Micro LED Displays," SID Symposium Digest of Technical Papers, pp. 520-523 (2020).