PRJ4-1
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Implementation of Projection Mapping System Using FPGA

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Keywords: geometric correction, free-from surface, mannequin, pipeline, cache circuit

ABSTRACT

We developed a system that uses separate devices for video output and video correction, to easily and inexpensively map projections onto 3D objects with free-form surfaces. An FPGA board was used as the correction device. Furthermore, we describe the details regarding the geometric correction circuit designed for the FPGA board.

1 INTRODUCTION

Projection mapping is a technique that maps video onto 3D objects. This technique basically measures the shapes of the 3D objects and performs geometric correction of videos based on the measurement results. Geometric correction of 3D objects composed of free-form surfaces is a highly complicated task requiring pixel-by-pixel correction. In this study, we developed a projection mapping system that simply and inexpensively maps videos onto 3D objects according to the demands of video creators. Our system consists of a geometric correction circuit designed on a field-programmable gate arrays (FPGA) board, and a program (written in OpenCV) that measures the geometric correction between the camera and the projector [1][2]. The developed system supports full HD resolution [3].

2 CONCEPT

Typical projection mapping methods use dedicated media servers or dedicated applications running on a personal computer (PC). Such methods require 3D data processing or fine geometric transformation. These methods are not fully automated, and are therefore laborious and time-intensive. Moreover, dedicated media servers are generally very expensive.

We devised two basic concepts. The first is alleviating the technical difficulties faced by video creators by eliminating the need for geometric transformation. Video creators prefer simple 2D images instead of complicated 3D data [4]. Our system uses a 2D image captured using camera for the sketch, and combines it with the geometric transformation measurement information from the projector-camera system [5][6]. Thus, it is possible to eliminate 3D data processing and the manual geometric conversion process. The second is to reduce the cost of projection mapping. Using these two concepts, we encourage video creators to actively participate in the world of projection mapping-based video expression, thereby contributing to the development of video culture.

It is difficult to simultaneously run a video production application and a geometric transformation application on a single PC. Therefore, we perform geometric transformation on another device. Further, we implement geometric transformation in pixel units using an FPGA board with video input and output. Because geometric transformation is performed on a different PC from the one used for video output, video creators can conveniently and easily work with their favorite video production applications.

3 DESIGN OF FPGA BOARD

3.1 FPGA Board Specifications

We chose the Nexys Video (Digilent, Inc.) FPGA board [7] owing to its wide availability and moderate price. This board has an HDMI sink, HDMI source port, and SDRAM, suitable for our design. The SDRAM has a memory bandwidth of 1600 MB/s. The FPGA chip on the board is a Xilinx Artix-7. The board costs approximately $500.

3.2 Geometric Correction Data

A single pixel data of the geometric correction data for full HD resolution is composed of 11-bit x-position and 11-bit y-position. The number of correction data is equal to the number of pixels in one screen. As shown in Fig. 1, the correction data are inputted to the FPGA board using the HDMI sink port as 24-bit pixel data. All pixels of the image outputted from the FPGA board are replaced with the pixels of the input image at the position indicated by the corresponding correction data. If all bits of the correction data of a pixel are 0 or 1, it is the mask data. The pixels corresponding to the mask data are automatically set to black.

3.3 Geometric Correction Circuit

Fig. 2 shows the block diagram of the geometric correction circuit. The AXI4 is a data transfer standard

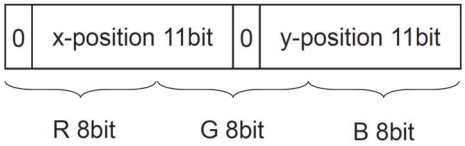


Fig. 1 Geometric correction data

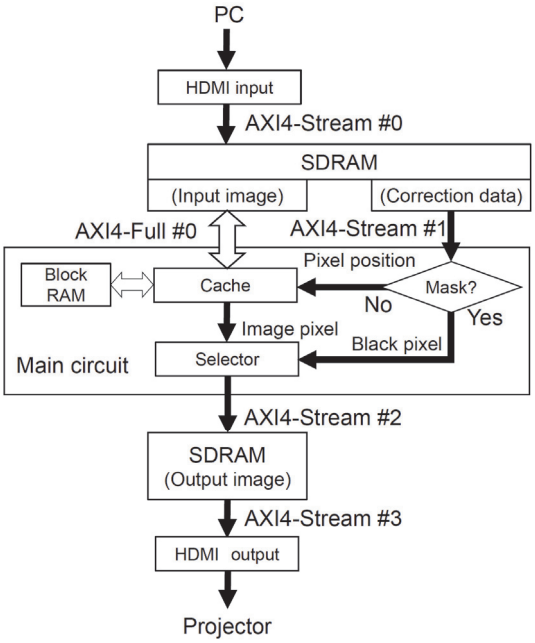


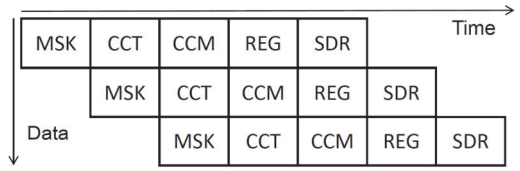
Fig. 2 Geometric correction circuit

between circuit blocks in an FPGA; AXI4-Full is capable of burst transfer. The AXI4-Stream is used to transfer continuous data such as images and audio [8].

The AXI4-Stream #0 stores the input image in SDRAM, and the AXI4-Stream #1 inputs the correction data to the main circuit. If the geometric correction data are mask data, the output pixels will be black. If the geometric correction data are position data, the output pixels will be the input image at the position specified by the correction data through the cache circuit and AXI4-Full #0. The AXI4-Stream #2 writes the output image outputted from the main circuit to the SDRAM.

3.4 Main Circuit

As shown in Fig. 3, the main circuit is pipelined to avoid the reduction of geometric correction throughput. The pipeline process involves five circuits. If the output pixel is determined at each stage, the later circuits send the output pixel unchanged. The main circuit incorporates a cache circuit that changes the random access to the SDRAM in



SYM.	Processing
MSK	Mask data ? Yes, black pixel → pixel data
CCT	Cache table access for checking cache hit
CCM	Cache hit ? Yes, cache data → pixel data
REG	Register array hit ? Yes, one of register array data → pixel data
SDR	SDRAM access : one of SDRAM burst read data -> pixel data, SDRAM burst data → Register array data , Update of cache table and cache data, The pipeline is paused during SDRAM access

Fig. 3 Pipeline of the main circuit

1-pixel units to burst access; the burst access length is 32 pixels. The block RAM in the FPGA chip is the cache memory. Because block RAM cannot read data in 1 clock, each circuit has a more detailed pipeline processing. The data from several clocks ago are not contained in the cache memory; therefore, the data read by burst access are stored in the FPGA register array. This register array is used as a primary cache. Because the number of SDRAM access clocks is not constant, the pipeline stops when the SDRAM is being accessed.

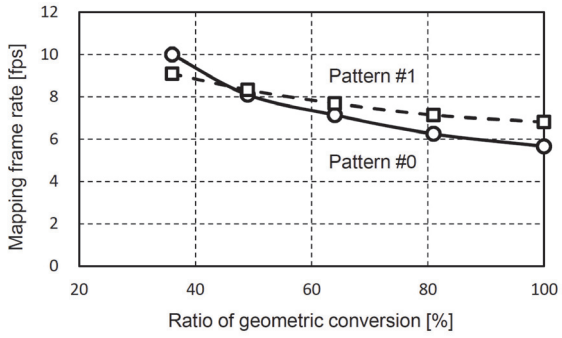
The size of the cache memory is approximately 130 000 pixels, which is approximately 1.6% of all pixels. The block RAM utilization of the FPGA chip is 46 %.

3.5 HDMI Input and Output

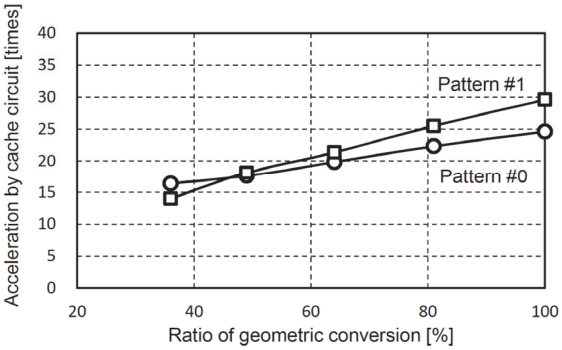
One pixel is set to 32 bits owing to the convenience of memory address calculation during geometric correction. A memory transfer rate of approximately 500 MB/s is required for full HD resolution at 60 fps. Because five channels are available for access to the SDRAM, a memory bandwidth of at least 2500 MB/s is required to run the circuit at 60 fps. However, the memory bandwidth of the used FPGA is insufficient. Image transfer from SDRAM to HDMI output is prioritized to ensure that the video output to the projector is uninterrupted. The video input circuit is designed to update the input video once for every two frames.

4 PERFORMANCE MEASUREMENT

Fig. 4 shows the frame rate of the designed FPGA circuit. Two types of geometric transformation pattern



(a) Frame rate



(b) Acceleration by cache circuit

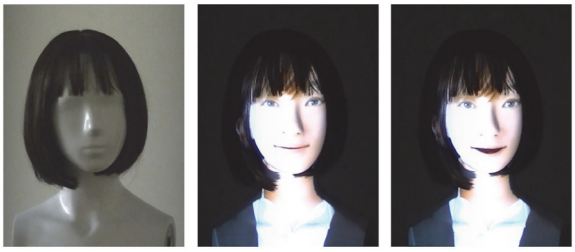
Fig. 4 The results of frame rate measurement

were used for the measurement. Pattern #0 is geometrically transformed to the same position; Pattern #1 rotates Pattern #0 by 90°. Because the processing speed differs between the mask part and the geometric conversion part, the ratio of geometric conversion is shown on the horizontal axis. As shown in Fig. 4(a), the frame rate is 6–10 fps. Fig. 4(b) shows that the acceleration by the cache circuit is 15–30 times [3].

5 DEMONSTRATION

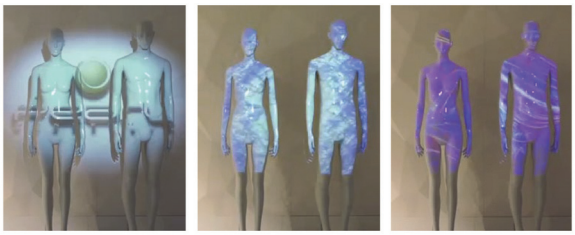
Fig. 5 shows the three demonstration tests conducted in this study. In the demonstrations, a mannequin was used as the 3D object with free-form surface. A real wig was used as the mannequin's hair. When we used a video of a woman speaking (Fig. 5(a)), the mannequin's mouth did not move, but the viewers perceived it to be moving. Furthermore, the video conversion speed was sufficient. The mannequin's hair was a real wig. Geometric correction measurements were performed without the wig [9].

The second demonstration is of the mannequin changing clothes, as shown in Fig. 5(b). The demonstration was held at the Digital Signage Japan 2019, in cooperation with Pearl Mannequin Co., Ltd. In the second demonstration, the mannequin wore a white T-shirt and white pants. The projector was mounted at a height that avoided disturbing the viewers. The adjustment work, including geometric correction measurement at the exhibition site, required approximately 10 min.



(a) Woman speaking

(b) Mannequin changing clothes



(c) Fantastic mannequins

Fig. 5 Demonstrations using mannequin

The third demonstration involves fantastic mannequins, which were installed in the Pearl Mannequin's Tokyo showroom. As shown in Fig. 5(c), the videos of the background wall and the mannequins were seamlessly connected by geometric correction. Various image patterns were projected onto the mannequins. The projector was mounted on the ceiling to avoid disturbing viewers. An inexpensive media player was used as the video output device.

6 DISCUSSION

The evaluations of the demonstration tests were well-received. We were able to perform the demonstrations with a short setup time. This is close to the realization of our concept. The viewers did not complain of the low fps caused by the slow changes in the video content. Our future work will be the implementation of 60 fps projection system, for which two methods are possible: (a) to use an FPGA board with a high memory bandwidth, and (b) to eliminate the memory transfer process in the mask part. The latter is a technology required to support 4K or 8K resolution.

7 CONCLUSIONS

We demonstrated the implementation of geometric transformation in projection mapping using an FPGA board. Our system supports full HD resolution, but the conversion speed is approximately 10 fps. Although the conversion speed was insufficient, the implemented cache circuit functioned effectively. The demonstration tests using mannequins showed that attractive video contents can be projected onto free-form surfaces in a short time.

Our future work is to improve the convenience of the measurement program of the system for geometric corrections.

ACKNOWLEDGMENTS

This work was supported by JSPS KAKENHI Grant Numbers JP26350025 and JP20K12536. In addition, authors would like to thank Pearl Mannequin Co., Ltd. for providing the opportunity to demonstrate the system.

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