PRJ6-1
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A Novel 3DLP 8K DLP Video Processor

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Keywords: Super Resolution, DLP Micro-mirror Array, High Frame Rate

ABSTRACT

A technique to achieve both an ultra-high resolution and high frame rate projection system is described using standardized control components for a digital light processing system. In addition to rendering higher resolution images, high speed systems can be used to minimize latency and provide other augmented reality features.

1 INTRODUCTION

Pixel-shifting methods have been used in various display technologies such as LCOS, LCD and DLP. The fast switching properties of DLP have provided video processing and feature flexibility that have been enhanced over the last 15 years. However native 4K DLP chipsets were not designed for pixel shifting, thus preventing a straightforward method to achieve higher resolution systems.

1.1 HISTORY

The first use of using the high switching speed of DLP devices to achieve high resolution was introduced in rear-projection consumer displays [3]. Subsequent improvements in algorithms and techniques were introduced and released in single chip solutions using a two-position pixel-shifting solution [1]. The first 4K class solution was achieved with a 4-position pixel shifting method in high brightness three-chip solutions [4]. The technique was then incorporated in standardized chipsets and offered in 1-chip DLP solutions which are available today.

1.2 ACHIEVING 8K

While Texas Instruments offered native 4K devices, the nature of the driving electronics were optimized for cinema content and supported up to 120 Hz frame rates for certain digital film releases [2]. Extending the capabilities of the available driving electronics was required to support higher resolutions using pixel shifting methods.

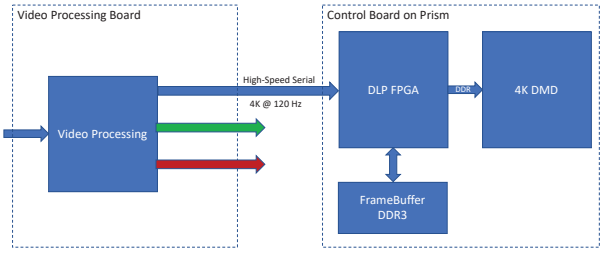

Figure 1 Standard 4K DLP Block Diagram

2 METHOD

Figure ***1*** depicts the existing standard TI 4K electronics architecture, which is limited to 120 Hz frame rates. Not only did we need to extend this to support 8K display resolutions, but practical considerations of PCB size, EMI and cost were also required to be considered for a viable commercial solution.

A block diagram of our system architecture is shown in
Figure **2**. 8K data is provided to a sub-frame processing FPGA. High-speed serial data connections were utilized in order to minimize the FPGA package size.

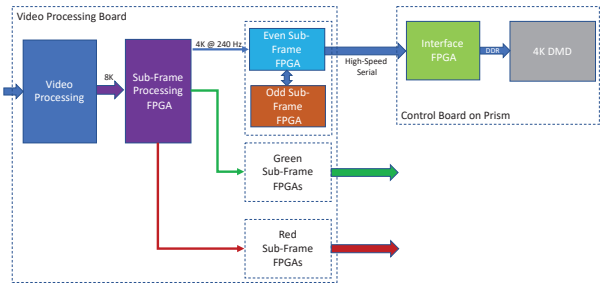

Figure 2 8K Block Diagram

The incoming video is processed and written to a sub-frame FPGA frame-buffer, allowing individual sub-frame data to be read out to the native 4K resolution of the DMD device. For 60 Hz 8K video formats, 4 sub-frames are created and rendered at 240 Hz. Data for each color is sent to a single “even-frame” FPGA which processes even sub-frame data and simultaneously sends odd-frame data to an auxiliary FPGA. The “even” FPGA takes the “odd-frame” DLP data and merges it to send out to 4K DMD. The Texas Instruments 4K control block, provides the same core embedded in their standard

FPGA solution.

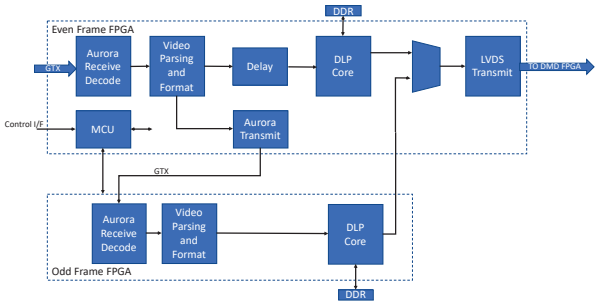

Figure 3 Odd/Even FPGA Functional Details

Implementing two FPGA and associated DDR memory sub-systems were not physically feasible on a compact prism board. Neither was driving each DMD from a main control board, since the 1.38" 4K DMD relied on a wide, low-voltage DDR interface. This was solved by reformatting the DMD control signals using differential signaling. This was retimed and applied to the DMD with a relatively small and relatively inexpensive FPGA located on each prism assembly PCB.

3 4-POSITION PIXEL SHIFTING

Image data is applied and then is resampled in a manner to create subframe images. This corresponds to the position of the optical actuator which alters the image location on the screen by a ½ pixel horizontally or vertically. Various methods can be applied during the resampling process to optimize the perceived image and to account for other downstream image processing such as spatial-temporal multiplexing, pulse-width modulation, and additional blurring due to motion of the actuator and projection optics.

Meerleer [7] describes how LCD and LCOS systems can upconvert by a factor of 2 using a single ½ pixel shift and DLP projectors achieve an upconversion factor of 2.25. Similarly, we can describe that a DLP 4-way solution creates 2x the number of subframe pixels thus creating a 4x upconversion factor.

Figure 4 illustrates the theoretical highest perceived resolution of the sub frames if the sub-frame phase are at their maximum frequency for each phase. While the 2-position method has a superior performance along 45° degree axis, the 4-position provides an overall superior 2 dimensional result.

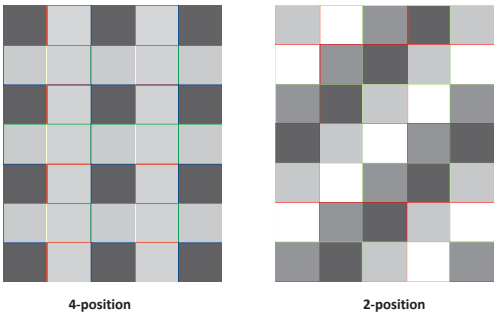

Figure 4 Subpixel Method Comparison

Another interesting effect of pixel pitch geometries is a smaller fill-factors provide improved perceived sharpness of the image. The MTF of a pixel (ignoring other optical effects) is

$$MTF = sinc(\mathrm{W})^2 * comb(\mathrm{S})^2$$
$$\mathrm{A} = \pi f w$$
$$\mathrm{S} = p f$$

Where f is the pixel spatial frequency, w is the width of the pixel, and p is the pixel pitch. A larger gaps between pixels provides a higher frequency passband by shifting the *sinc* null to a higher spatial frequency. This increased passband can be optimized based on the MTF of the specific projection optics using various sharpness enhancement methods.

4 DISCUSSION

In addition to the electronics solution, we also developed various PWM sequence solutions necessary for the sub-frame creation as well as optimized PWM solutions for 4K operation at 240 Hz. Due to the transition time between sub-frames, 8K PWM solutions were more challenging to achieve good overall image quality compared to higher frame rate modes that did not require the use of pixel shifting.

Thus far, we have only considered static imagery and avoided degradation of image blurring, which is induced by the human eye tracking an moving object using PWM methods for grey-scale creation.

Using sub-frame generation generally requires use of the entire display time to render the 8K image with a complete sufficient grey-scale. This is limited by the overall rate the DMD can be loaded (limited both by the loading speed of the DMD interface and the associated read-out speed of the bit-plane frame buffer). This prevents the use of motion-blur reduction methods whereby the time an image is rendered by PWM is reduced to ¾ (12.5 ms) or even ½ (8.33 ms). Bandwidth improvements of future generations will enable enhanced motion reproduction in high performance applications such as simulation systems and methods while realizing visual resolution enhancement [8][9].

5 CONCLUSIONS

Through the use of high-speed interface methods available with advances in FPGA technology, a substantial improvement in visual resolution was achieved using an existing DLP chipset. In addition, high frame rate capability is also available to support emerging AR and VR applications. For example, VR data could be injected into one of the sub-frames prior to DLP formatting.

Gaming and E-sports users desire higher temporal resolution and prefer 4K images at 240 Hz instead of 8K images at 60 Hz. This minimizes latency to the user, improves the viewers experience and reduces motion blurring [10]. Next generation GPU's are now capable of 240 Hz at 1080P and it seem clear that next generation solutions will support 4K @ 240 Hz. It will be interesting to see how content creators will take advantage of these new capabilities. Variable frame rate support will be developed to support the latest GPU solutions such as Nvidia GSYNC and AMD Freesync.

Industrial applications can also take advantage of these methods. Theoretically, this architecture could be expanded to support higher input data rates but are impractical to implement due to cost. A more general purpose high-speed interface DLP control chipset would expand the possible applications and users of 4K solutions.

The digital flexibility of DLP technology provides the necessary flexibility to create video processing solutions to meet a wide variety of needs.

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