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Highly Compatible Low Temperature Polycrystalline Silicon Oxide Technology for High-resolution Display Backplane Applications

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ABSTRACT

In this work, we demonstrate the low-temperature polysilicon oxide (LTPO) thin film transistors (TFTs) technology to realize the inverter with hybrid complementary TFTs for high resolution pixel array applications. The inverter with a high gain of ~11V/V and high noise margin was achieved successfully.

1 Introduction

The demands for ultra-high resolution have become a major trend of flat panel display (FPDs) technology. In order to increase the display resolution, the pixel size and transistors within (switching, driving transistor) need to be scaled down to achieve low signal propagation delay, low power consumption, and high resolution. Several ideas came up to address above problems by combining different kinds of TFTs, such as the integration of the high mobility of low temperature poly silicon (LTPS) TFTs and the amorphous oxide semiconductor with low leakage current and good uniformity [1-2]. In recent, the low temperature polysilicon oxide (LTPO) technology is considered as the promising technology to achieve the above features. The LTPO architecture was also well demonstrated by Apple at 2019 SID symposium [3]. The AOS TFT and LTPS TFT features low leakage current for switch and high driving capability for driver applications, respectively, in organic light-emitting diode (OLED) displays. Also, LTPO technology can be expected to integrate the manufacture of both of pixel arrays and periphery circuit for the system on panel (SoP) applications, which can effectively reduce the cost in the panel fabrication. However, it is undeniable that the LTPS TFTs and AOS TFTs aren't physically and characteristically compatible. The most critical challenge in the LTPO architecture is the lower mobility of AOS TFT compared to the LTPS TFT, leading to the required design of large gate width for the circuit with higher operation voltage. Not only will the size of AOS TFT and LTPS TFT be mismatched, it will also reduce the display resolution and consume more power. Thus, the development of indium-based AOS materials for high mobility transport are crucial. Besides, it is necessary to release the issues on the electrical uniformity of LTPS TFT originated from the uneven distribution of Si grain boundaries; otherwise, display quality degradation is prone to occur. To sum up, the optimization of the two hybrid semiconductor-based TFTs is indispensable for the successful development of LTPO technology.

In this work, we demonstrate the hetro-semiconductor TFTs and resultantly the hybrid complementary inverter, composed of high-mobility indium-based AOS TFT and p-channel poly-Si TFT for TFT display backplane applications. The inverter with a high gain of and high noise margin can be achieved successfully.

2 Experiment

Figure 1 shows the schematic of LTPO hybrid complementary TFTs (HC-TFTs) consisting of AOS TFT and LTPS TFT. The fabrication procedure of LTPO HC-TFT is p-channel ploy-Si TFT completed first and then followed by the integration of n-channel indium-based TFT. Firstly, the SiO_2 was grown by the furnace to simulate the glass substrate. The a-Si thin film layer was deposited as the active area of p –channel poly-Si TFTs and then recrystallized to poly-Si by the solid-phase crystallization (SPC) method. Following the deposition of high dielectric constant HfO_2 by atomic layer deposition (ALD) as the gate insulator, the molybdenum (Mo) was deposited by DC-sputtering to be the common gate electrode of HC-TFTs. The HfO_2 layer was deposited by ALD again acting as both of the passivation layer of p-channel poly-SI TFTs and the gate insulator of n-channel indium-based TFT. After the deposition of indium-based oxide as the n-channel TFTs channel, the Mo source/drain (S/D) electrodes was defined by lift-off process. Finally, gate electrodes and the drain electrodes of both of p-channel and n-channel TFTs were connected by the interconnection metallization process, and then the HC-TFT was completed in this work.

3 Results and Discussion

The HC-TFT is considered to be the promising technology as the driving circuit and pixel array for the SoP application. As shown in Fig.2, the transfer curves (I_D-V_G) of n-channel indium-based oxide TFT are exhibiting the superior electrical characteristics. The high field effect mobility (μ_{FE}) of ~ 20 cm^2/V-s, sharp subthreshold swing (S.S.) of ~70 mV/dec. and large on-off current ratio (I_{ON}/I_{OFF}) ratio of 10^8 are achieved. Figure 3 shows the I_D-V_G curves of p-channel poly-Si TFTs, and

the μ_{FE} of ~ 20 cm^2/V-s, S.S. of ~140 mV/dec. and large I_{ON}/I_{OFF} current ratio of 10^6 are also achieved. The p-channel TFT and n-channel TFT are well compatible to be integrated into a inverter unit for the display periphery circuits due to its matching up electrical property. Figure 4 demonstrates the voltage transfer characteristics (VTC) of the inverter at V_{DD} = 0.5 V and the voltage gain of ~11 V/V.

4 Conclusions

In this work, we have successfully demonstrated the high-performance n-channel indium-based AOS TFT, which is compatible to be integrated with p-channel poly-Si to form the LTPO HC-TFTs. The LTPO HC-TFTs can be used to realize the inverter of logic unit, in which the symmetric VTC curve, high voltage gain and high noise margin have been achieved successfully. It is highly promising for the proposed LTPO technology to realize high-resolution pixel array and periphery display circuits, effectively reducing the manufacture cost and volume of display panels.

Acknowledgment

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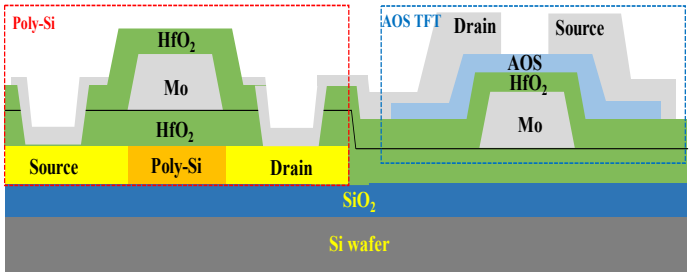

Fig.1 Schematic structure of LTPO Hybrid complementary TFTs (HC-TFTs).

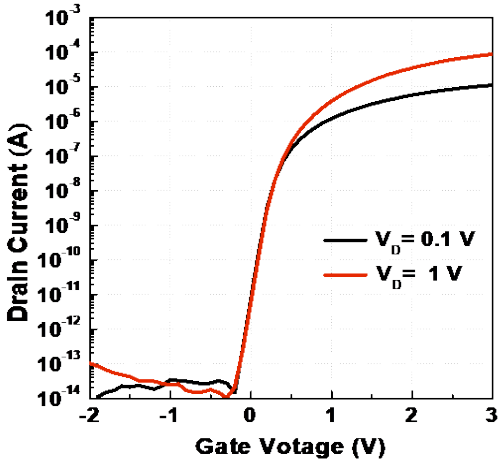

Fig.2 The transfer curve of n-channel indium-based oxide TFT.

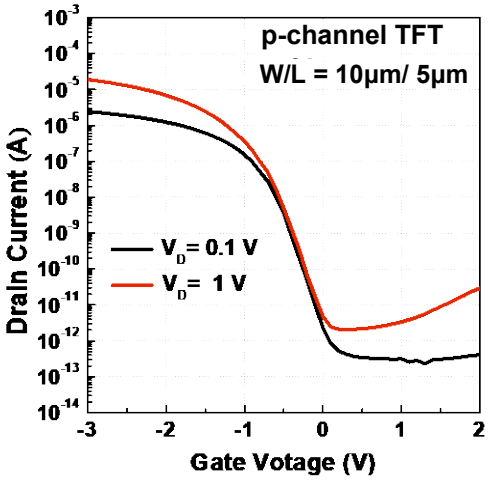

Fig.3 the transfer curve of p-channel poly-Si TFT.

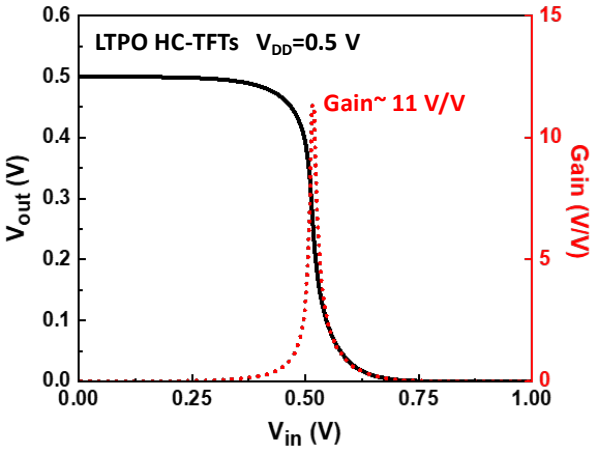

Fig.4 The voltage characteristic and voltage gain of inverter, consisting of LTPO HC-TFTs.