Internal Compensation by Offset Method for QHD OLED Display Using High Mobility Oxide TFT

Yong Ho Jang, Kwang Il Chun, Younghyun Ko, Uyhyun Choi, Min-Gu Kang, Hyung Joon Koo, Seung Chan Choi, Dae Hwan Kim, Jiyong Noh, Kwon-shik Park, JeomJae Kim and SooYoung Yoon

yhjang@lgdisplay.com
LG Display Co., Paju-shi, Gyeonggi-do, Korea
Keywords: internal compensation; offset method; QHD OLED; high mobility; oxide TFT;

ABSTRACT

A new internal compensation method for OLED display with high mobility oxide TFT is presented. The offset method can preemptively eliminate Vth-dependent voltage errors, ameliorating the mismatches after-sensing step. Fabricated 5.5-in. QHD OLED displays show improved uniformity.

1 Introduction

Since successfully adopted in large-sized OLED TVs, oxide TFTs have been paid increased attention [1, 2, 3]. Manufacturability of oxide TFTs on Gen. 8 or larger glass sizes, which is a major advantage over low temperature poly-Si (LTPS) TFTs, has motivated the development of more stable and higher mobility oxide TFTs aiming not only OLED TVs but also other application areas presently covered by LTPS TFTs.

While OLED TVs have begun with external compensation technique [4, 5], internal compensation schemes are preferable for small and medium sized OLED displays. Usually, high mobility comparable to LTPS is desirable for acceptable accuracy of compensation, which is is thought to be achieved by sufficient charging [6].

Recently, we have reported an internal compensation type 5.5-in. FHD OLED using high mobility oxide TFT [7, 8]. It was shown that when the threshold voltage deviation amounts to 2 V, the mismatch voltage after sensing step for FHD panel (1H ~8.6μs) can be reduced to 13 mV by accomplishing the mobility of 50 cm^2/Vs whereas it is as large as 250 mV with the mobility of 10 cm^2/Vs.

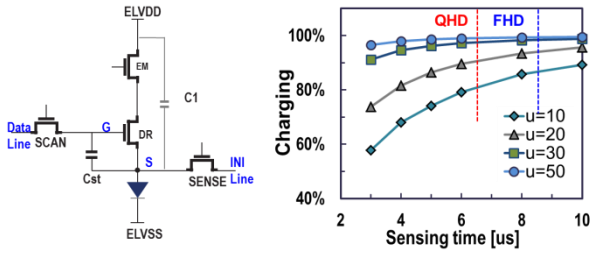


Figure 1. (a) Schematic diagram of the pixel circuit for in-pixel compensation, (b) Simulation of target voltage charging with time for various mobility of driving TFTs

When the resolution and/or frame frequency is higher, it is difficult to allocate sufficient amount of time for sensing, especially with pixel circuits of simple architecture.
In this paper, we present a new compensation scheme with shortened sensing time.

2 Conventional Compensation Scheme

Figure 1(a) shows the schematic of the pixel circuit for internal compensation adopting a source-follower architecture. V_{REF}-V_{INI} is initially set across C_{ST}. During the subsequent sensing step, the voltage of source node (S) of the driving TFT increases, while the gate node (G) is maintained at a constant voltage, V_{REF} of data line voltage with the SCAN TFT on. Consequently, the compensation voltage (V_C=V_{REF}-V_S) relating to the threshold voltage of the driving TFT is stored in C_{ST}. After data writing, the source node voltage changes so that the EL diode is biased to flow the same current as the driving TFT. More detailed description was reported in the previous work [7].

Panel specification

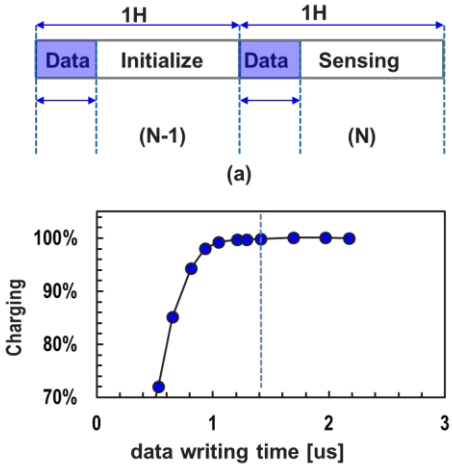
Resolution	QHD (1440 x 2560)
Screen	5.5-in.
Pixel Size	48 μm x 48 μm (2 subs)
PPI	538
Integration	SCAN & EM Driver with oxide TFT

Figure 2. QHD OLED panel using the offset method for accurate compensation

Figure 2 shows the photograph of an OLED panel used in the present work. The specification is the same as ordinary QHD OLED panels for mobile phones.

Details about technical challenges in design and fabrication process will be presented somewhere else.
For 60 Hz QHD display, both sensing and data writing is done within 1 H of ~6.5 us in case both voltages for data and ref are supplied through the same data line as is

seen in Figure 3(a). The measurement of luminance shows that charging of data voltage becomes apparently saturated after ~1.4 us. Therefore, around 5 us is available for sensing without deteriorating the data voltage.



(b)

Figure 3. (a) Schematic diagram of the data timing. Sensing and data writing is done within 1 H for the pixel circuit as in Fig.1. **(b)** Charging ratio vs. data writing time estimated by luminance measurement of a display panel

Figure 4 shows global uniformity (G/U) of luminance, representing uniformity of the measured luminance of more than dozens of local areas all over the display. The improvement of uniformity by increasing the sensing time slows down after rapid increase in the beginning, which indicates difficulties of getting better performance by only increasing sensing time. It also suggests that there exist other factors affecting the current variation.

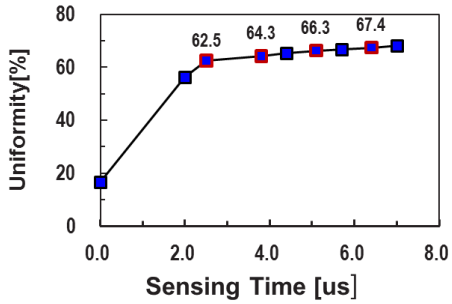


Figure 4. global uniformity (G/U) with sensing time

After sensing, the current of driving TFTs of two different pixels depicted as i-th and k-th can be put as

$$I_i = I_i(V_{i0} + \Delta V_i), \quad I_k = I_k(V_{k0} + \Delta V_k)$$
$$I_i(V_{i0}) = I_k(V_{k0}) = I_0 \qquad (1)$$

The Vth sensing is a process of sampling V_{i0} and V_{k0} respectively for each pixel such that Eq. (1) holds with consequential mismatches ΔV_i and ΔV_k. The mismatch voltage is largely dependent on the Vth of the driving TFT of each pixel.

The mismatch voltage and the relative deviation of current as known as coefficient of variation (C.V.) in statistics in the sensing step is obtained by approximate calculation as in Ref.[7], where we assumed the parallel shifted I-V curve for different Vth's, ignoring any probable formal differences.

$$\frac{-\Delta V_i}{\Delta V_{TH}} \cong \frac{I_0}{I_i(V_{initial})} \equiv \frac{1}{g(V_I)}, \quad \frac{\Delta I_i}{I_i} \cong -\frac{\ln 10}{S(V_{i0}) \cdot g(V_I)} \cdot \Delta V_{TH} \qquad (2)$$

Thus, the sensing errors do not fully account for the uniformity.

Figure 5 shows the spice simulation of mismatch voltages during internal compensation process of the source follower type pixel, giving the mismatch voltage after sensing (SEN), data writing (DW), and settling (STL) steps induced by Vth variation. The mismatch during DW and STL is attributed to capacitor coupling and comprises larger portion of the total mismatch voltage difference. The mismatch after each step shows negative linear dependence like

$$\Delta V_{Ti} \cong m \Delta V_i \quad (\cong -m' \Delta V_{THi}) \qquad (3)$$

The total mismatch voltage difference affecting the uniformity can be estimated to be 4 times larger than that just after sensing in our case.

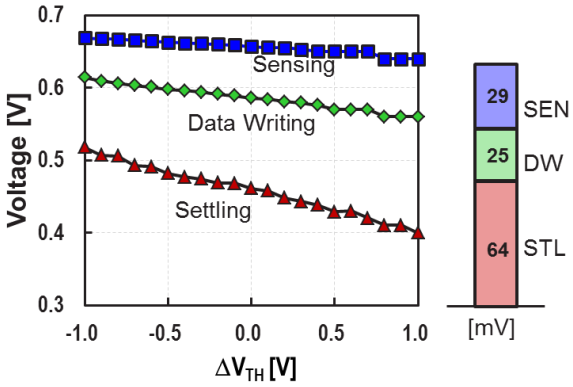


Figure 5. Total mismatch voltage by simulation vs threshold voltage variance after each step of compensation process. On the right is shown the net mismatch voltage produced during each step when ΔVth ranges between -1V and 1V.

3 Compensation by Differential Offset Method

We have come up with a new compensation scheme which can eliminate the voltage errors including after-sensing steps. The new scheme exploits linear dependence of mismatch voltage on Vth. The scheme is

equipped with the offset voltage forming period where the voltage at the gate node of the driving TFT is designed to increase after sensing. This happens when the gate node gets disconnected with the data line and the source node voltage increases as the offset forming current is charging the capacitors attached to the source including C1 and EL cap as in Figure 1.

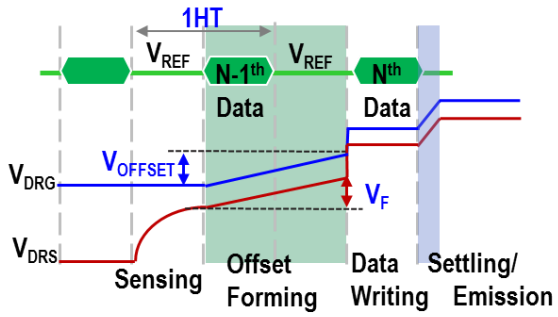


Figure 6. Schematic timing diagram of node voltages of a driving TFT during the new internal compensation process including offset (voltage) forming step.

After the offset forming step, the source node voltage is increased by V_F and the consequent increase of gate node voltage is V_{OFFSET} as in Figure 6.
Each pixel renders a different offset forming current depending on the respective mismatch voltage ΔV_i set up during sensing process. For the forming time t_F, the i-th pixel has

$$V_{offset} = \eta V_F = \eta \frac{1}{C} I_i(V_{i0} + \Delta V_i) t_F$$
$$= \eta \frac{1}{C}\left[I_i(V_{i0}) + \frac{dI_i}{dV}\Delta V_i + \frac{d^2 I_i}{2dV^2}(\Delta V_i)^2 + o(\Delta V_i)^3 \right] t_F \quad . \ (4)$$

Here, η is from coupling of the gate node to environments.
At the subsequent data writing step, in which the change of data line voltage is transferred to the storage cap, an extra voltage of $-\alpha V_{OFFSET}$ is added to each pixel, where α is in consideration of the transfer ratio.
For compensation's sake, the optimal offset forming time (t_F) is chosen to satisfy the condition,

$$\Delta V_{Ti} = m\Delta V_i = \alpha\eta \frac{1}{C}\frac{dI_i}{dV}\Delta V_i t_F \quad . \ (5)$$

Therefore, the mismatch is mostly cancelled and the second order term of ΔV_i dominates the deviation.
Considering the simple case of applying the data voltage equal to V_{REF}, the current at the emission step has the form of

$$I_i(V_i) = I_i(V_{i0} + V_0 + \delta V_i) \quad . \ (6)$$

Here, V_0 is constant for all pixels and δV_i is the mismatch voltage reduced as follows,

$$V_0 = -\alpha\eta \frac{1}{C} I_i(V_{i0}) t_F, \quad \delta V_i = V_0 \frac{d^2 I_i}{2 I_i dV^2}(\Delta V_i)^2 \quad (7)$$

When the I-V equation approximately has the exponential form with inverse slope S, the resultant current variation is reduced as follows,

$$I \cong I_i(V_{i0}) 10^{\left[-\frac{m}{\ln 10} - \frac{m}{2}\ln 10 \left(\frac{\Delta V_i}{S} \right)^2 \right]} \quad (8)$$

On the while, with the conventional compensation method, the current becomes

$$I \cong I_i(V_{i0}) 10^{\left[m\frac{\Delta V_i}{S} \right]} \quad . \ (9)$$

From Eq. (8) and (9), coefficient of variation (C.V.) in statistics can be obtained roughly as

$$CV_{OFFSET\_METHOD} \cong \frac{1}{2m}\left(m\frac{\ln 10}{S}\Delta V_i \right)^2, CV_{CONV} \cong m\frac{\ln 10}{S}\Delta V_i \quad . \ (10)$$

The current variation can be reduced to the second order of the initial sensing error, ΔV_i.
The offset forming current is no other than the current at the end of sensing step and can be named sensing current. The sensing current is seemingly saturated as sensing time increases, as is consistent with Figure 1 and Figure 7.
This means the optimal time for sensing can be made smaller in the new compensation scheme by choosing suitable offset forming current

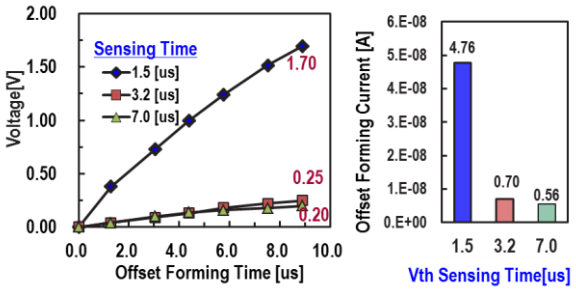
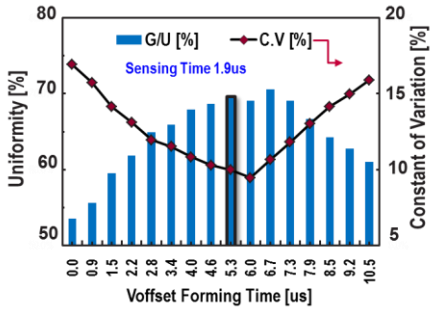
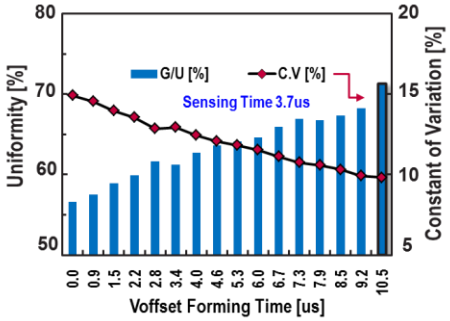


Figure 7. Estimated offset voltage vs offset forming time from measurements with different sensing time. The offset forming current on the right was obtained from the values at offset forming time of 8.6 us.

Figure 8 (a) and (b) show that the optimal offset forming time depends on the sensing time. With shortened sensing time, the optimal offset voltage can be built for shorter offset forming time as the offset forming current is increased. The mismatch voltage after shortened sensing becomes correspondingly larger.
The relative deviation of current (C.V.) with the offset method compensation as a function of initial Vth variation is visualized as contour maps in Figure 9.



(a)



(b)

Figure 8. Uniformity vs offset voltage forming time measured for a display panel with two different sensing time.

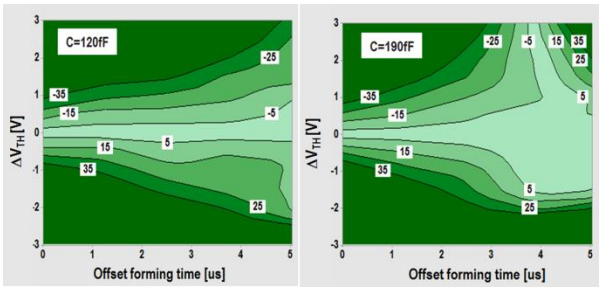


Figure 9. Contour map of C.V. of driving current spice simulated with two different storage caps.

With a fixed Vth variation, C.V. initially decreases as offset forming time is increased. Near the optimal forming time the error becomes markedly small. Further increase in forming time increases the deviation again with the sign change. The larger storage capacitance gives shorter optimal time, as is consistent with effect of the larger transfer rate (α) as in Eq. (5).

Figure 10 shows the effect of new compensation method. m=1 just after sensing step, and increases to around 4 as seen in Figure 5. When the coefficient of ΔV_i is estimated to be about 30, the uniformity with the conventional compensation can be 60% with ΔV_i= 13 mV, which can be attained with smaller initial Vth variation in panels. In this case, according to Eq. (10), the uniformity can be up to over 90% with the offset method .

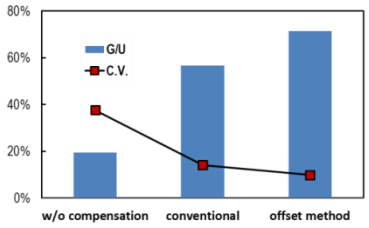


Figure 10. Improvement of uniformity by the new compensation scheme.

Two possible sources of errors can be conjectured for expounding the overall small numbers of uniformity in this case. First, there can be variation in optimal t_F in spite of the formal universality. Second, other factors yet to be compensated remains such as S-factor variation etc.

4 Summary

Introduction of a new internal compensation scheme by differential offset method was presented with the improved uniformity of fabricated 5.5-in. QHD OLED display with high mobility oxide TFT. The new method was devised to preemptively eliminate Vth-dependent voltage errors especially that occurs during the settling step. This can be a way to overcome the disadvantage of source follower type pixel circuit.

References

[1] J. U. Bae et al., “Development of oxide TFT’s structures,” in SID Symp. Dig. Tech. Paper., vol. 44, pp. 89-92 (2013).

[2] C. Ha et al., “High Reliable a-IGZO TFTs with Self-Aligned Coplanar Structure for Large-Sized Ultrahigh-Definition OLED TV” SID’14 Dig., pp.1020-1022 (2015).

[3] K-S Park et al., “Development of High-Mobility, High-Stability Oxide TFTs”, ITC (2016).

[4] J.-S. Yoon, et al., “ 55-inch OLED TV using Optimal Driving Method for Large-Size Panel based on InGaZnO TFTs” SID’14 Dig., pp. 849-852 (2014).

[5] H.-J. Shin et al., “Technological Progress of Panel Design and Compensation Methods for Large-Size UHD OLED TVs” SID’14 Dig, pp.720-723 (2014).

[6] R. Chaji et al., “LTPS vs Oxide Backplanes for AMOLED Displays: System Design Considerations and Compensation Techniques” SID’14 Dig., pp.153-156 (2014).

[7] Y.H. Jang et al.,” Internal Compensation Type OLED Display Using High Mobility Oxide TFT” SID’17 Digest, p.76 (2017)

[8] D.H. Kim et al., “Gate Driver Circuits for Internal Compensation Type OLED Display with High Mobility Oxide TFT” SID’18 Digest, p.40 (2018).