SI-Aware Design Considerations for Flexible Channels on High-Speed Intra-Panel Interfaces in 8K TV Applications

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ABSTRACT

Although the signaling channels on FPC cable, FFC, and COF package are relatively short in the entire system of large-size TV modules, they can be a bottleneck that determines the overall signal quality in the system or can be of a great help for better eye opening at the receiver side of a driver IC. This work analyzes the channel characteristics for signaling traces on FPC cable, FFC, and COF package on signal integrity perspective, and suggests design guidelines for better signal quality at the input stage of source driver IC in high-speed intra-panel interface system of 8K TV applications.

1 Introduction

Recent advances in large-size TV applications toward 8K (7,680×4,320) resolution require a few Gbps signaling in intra-panel interface due to not only the high resolution but also high-refresh rate and precise color representation. In case driving an 8K panel of 120Hz frame rate and 10-bit color with 960ch source driver ICs (S-ICs), required data rate per S-IC becomes about 7Gbps. The customer's desire for more natural and vivid visual experience is requiring the ever-increasing development of power and signal integrity technology to operate at much higher frequencies, however, the intra-panel interface system suffers from a lot of factors that limit high-speed signal transmission [1].

There can be found that various flexible channels such as FFC (Flexible Flat Cable), FPC (Flexible Printed Circuit) cable, and COF (Chip On Film) package are used in large-size LCD TV modules as shown in Fig. 1. Besides the large panel size, the curved design of TV or monitor sets made it necessary to separate the source PCBs into more than three or four, and thus, more FPC cables are required to connect the separated source PCBs to each other. Moreover, the system sometimes needs a longer FFC due to the variations in the placement of TCON (Timing Controller) and SoC (System on Chip) boards in TV sets.

It is well known that interconnection discontinuities in electrical signal paths caused by these flexible cables and connectors are the hurdles in high-speed signal transmission because they might be the sources of electrical noises that make the high-speed signaling difficult [2]. Therefore, when designing a system in which high-speed signals are transmitted, impedance matching and crosstalk mitigation should be seriously taken into account from the design stage. However, the flexible channels have considerable limitations in electrical noise management due to their physical and structural characteristics. For example, compared to PCBs, the flexible channels are difficult to control impedance because they have much thinner cross-sectional structure with single layer. Also, due to the limited interconnection area, the interconnection density is very high, thus, crosstalk can be significant.

This work analyzes the characteristics of high-speed signaling channel on signal integrity (SI) perspective of impedance matching and crosstalk for flexible channels such as FPC cable, FFC, and COF package. Also this paper suggests the design guideline to obtain better signal eye opening at the receiver side of the input stage of S-IC.

2 Design Considerations of Flexible Channels

2.1 FPC (Flexible Printed Circuit) Cable

Fig.1 shows an example of the half-side of TV module to describe the intra-panel interface system architecture as well as the placement of the flexible channels, where it has a LCD panel with 75-inch, 8K resolution, 1G1D pixel structure, 60Hz frame rate, and 8-bit color depth.

Firstly, SI performance was reviewed for three types of FPC cable design which tried to be designed with the matched impedance of differential 100Ω and similar crosstalk level. Fig. 2 shows their physical design differences. This experiment was done with the FPC cables which were used for 4K/120Hz TV module, however, the results are applicable to 8K/60Hz TV

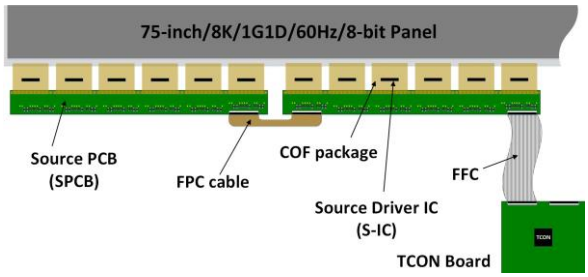
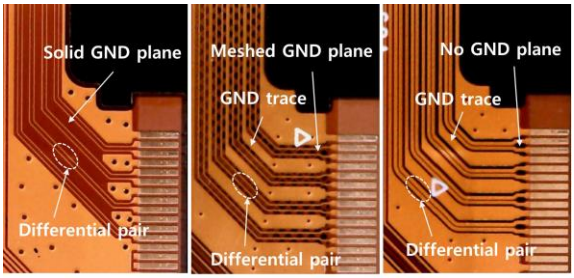


Fig. 1 An example of TV module (half-side) which has a panel with 75-inch/8K/1G1D/60Hz/8-bit color.



(a) FPC type A (b) FPC type B (c) FPC type C

Fig. 2 Three types of FPC cable, (a) two-layer with solid GND plane (Type A), (b) two-layer with meshed GND plane (Type B), and (c) single-layer FPC cable (Type C).

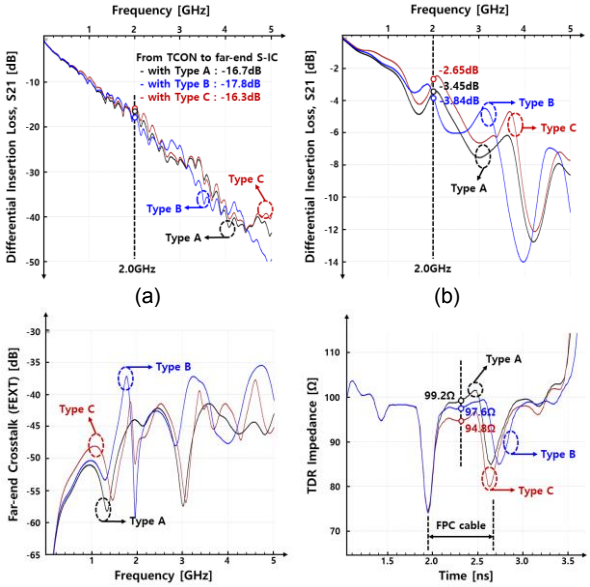


Fig. 3 Measured characteristics, (a) differential insertion loss of entire channels used in this analysis, (b) differential insertion loss of FPCs, (c) far-end crosstalk (FEXT) of FPCs, and (d) differential TDR of FPCs.

system because both cases have the same data rate and the number of differential pairs is sufficient to fully observe the crosstalk effect. FPC cable type A and B shown in Fig. 2(a) and Fig. 2(b) have both two-layer structure with ground plane at bottom layer, but the type A has solid ground plane and the type B has meshed ground plane. The structure with meshed ground plane allows for easy control of impedance in FPCs with a thin dielectric thickness [3]. FPC cable type C shown in Fig. 2(c) has single-layer structure. At 2GHz, which is the frequency range of interest in 4Gbps signaling, the measured insertion loss of overall channel is obtained about -17dB as shown in Fig. 3(a), and loss differences for the three types of FPC cables are less than 1.2dB as shown in Fig. 3(b). It can be noted that it accounts for about more than 16%~22% of the total loss despite the significantly shorter length of FPC cable compared to the SPCB based on the

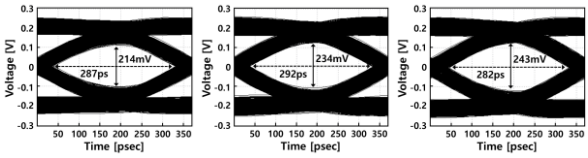


Fig. 4 Transient simulation results using measured channel model, (a) type A, (b) type B, and (c) type C.

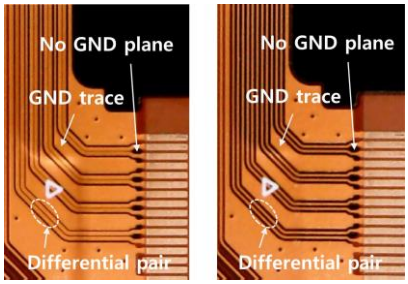
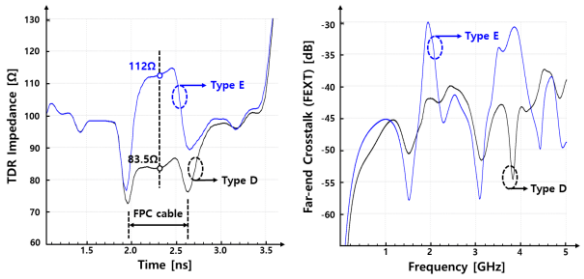


Fig. 5 Additional two types of FPC cable, (a) type D and (b) type E.

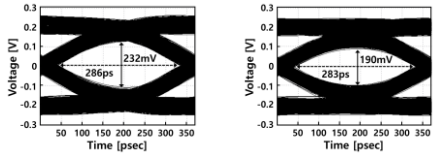
results of Fig. 3(a) and Fig.3(b). Although, to match 100Ω target impedance, signal trace widths and spaces for each FPC types are designed differently from each other depending on bottom ground layer structure and ground-shield traces between neighboring differential pairs as shown in Fig. 2, all three types of FPC cables show similar characteristics in FEXT and impedance as shown in Fig. 3(c) and Fig. 3(d), respectively. Transient simulation results using the measured channel models to compare eye opening performance for the three types of FPC cables are shown in Fig. 4. Data rate was assumed as 2.7Gbps for the driving condition of 8K resolution, 60Hz frame rate, and 8-bit color representation. Even the FPC cables with single-layer structure can provide good SI performance if impedance and crosstalk can be controlled well.

Secondly, two additional FPC types were reviewed to verify which one has a further impact on signal quality, between crosstalk or impedance. Fig. 5 shows the other two types of FPC with single-layer structure, type D and type E. To make the two types of FPC cables have different crosstalk characteristics, they are designed to have different dimension of signal trace width and space as well as the space between ground-shield trace and signal line. Type D and type E have -16.5% lower and +12% higher impedance, respectively, compared to the target impedance 100Ω as shown in Fig. 6. However, eye opening area of type D is 23% larger than type E, as shown in Fig. 7. Based on the crosstalk measurement result in Fig. 6(b), type D has similar crosstalk characteristics to the previous types, type A, B, and C, and it is observed that its peak level is about less 10dB than type E. Also, its eye height is similar to the waveforms in Fig. 4. Therefore, it can be addressed that



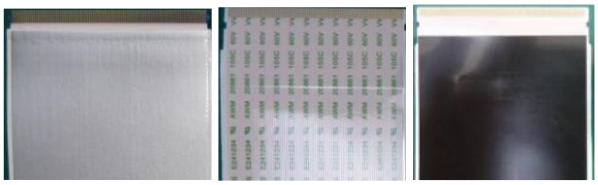
(a) (b)

Fig. 6 Measurement results, (a) differential TDR and (b) far-end crosstalk (FEXT).



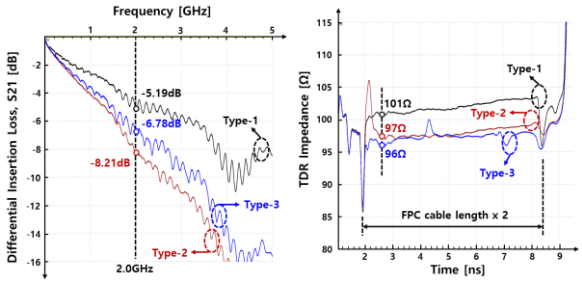
(a) (b)

Fig. 7 Simulated eye opening diagram, (a) Type D and (b) Type E.



(a) FFC type-1 (b) FFC type-2 (c) FFC type-3

Fig. 8 Three types of FFC for SI performance review, (a) Type-1, (b) Type-2, and (c) Type-3



(a) (b)

Fig. 9 Measured results, (a) differential insertion loss and (b) TDR impedance.

crosstalk mitigation is no less important than important impedance matching for better SI performance.

2.2 FFC (Flexible Flat Cable)

FFC length can be various according to the TV set structure from about 55mm to more than 1000mm. The longer the length become, the greater the insertion loss is, thus, it can be one of the causes of poor signal quality of the entire system as the FFC length increases. The electrical characteristics of FFC are dependent on the cross-sectional structure and dielectric materials [4]. Therefore, even though the length of FFCs are same, differential channel loss can be different from each other depending on the FFC provider. This work verified three types of FFCs made by three different FFC providers in terms of differential insertion loss and characteristic impedance. Fig. 8 shows photographs of the three types of FFCs. One is newly made to have low-loss characteristic for high-speed signaling more than 4Gbps which is represented as type-1 in Fig. 8(a), and the others are conventional FFCs which were applied to mass production which are noted as type-2 and type-3 in Fig. 8(b) and Fig. 8(c), respectively.

Fig. 9 illustrates the measurement results of differential insertion loss and TDR impedance. Type-1 shows the best performance compared to the others on both characteristics, insertion loss and impedance. Even if the differential impedance of all FFCs are within the range of design margin, which is less than about 5Ω differences (100Ω±10%) as shown in Fig. 9(b), conventional ones have much bigger loss than the new one. This performance was able to be obtained from adopting low dielectric loss insulation material to enhance transmission characteristic performance of a cable. It is obviously best to choose an FFC with the least insertion loss, but changing dielectric materials or cross-sectional structure can result in production cost increase. Therefore, in most cases, the FFC has to be selected considering cost and performance as well as target application, operating speed, and TX/RX equalization capabilities, etc.

2.3 COF (Chip-On-Film) Package

Fig. 10 shows a micrograph of S-IC input side of COF package on top view. There are high-speed differential signal pairs for point-to-point intra-panel interface, and the trace length of the differential pairs is about more than 11mm from input pad on SPCB to the bump at S-IC. This long trace introduces parasitic inductance, which can be demonstrated by the impedance simulation result with the s-parameter model extracted from the physical design in Fig. 10 by using Ansys HFSS showing a plot that tends to increase with frequency as shown in Fig. 11.

It is known that, for high-speed signal input stages of ICs beyond GHz, the parasitic capacitance due to electrostatic discharge (ESD) protection circuitry is expected to be in a few fF order because it can degrade the signal integrity of the system [5]. Display set or module makers require that IC vendors provide around ±10kV HBM ESD level for the open-cell business model in flat panel displays. For this reason, it is very difficult to reduce the parasitic capacitance of ESD protection circuitry meet the customer's requirements. In case of 180nm fabrication process which is generally used to fabricate the display driver IC (DDI) for TV applications, it is common that parasitic capacitance of the ESD protection circuitry is in a few pF.

But, if we can compensate the parasitic inductance due to the COF trace with the parasitic capacitance of

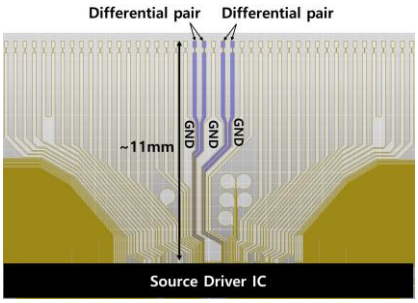


Fig. 10 Top view of micrograph of COF package.

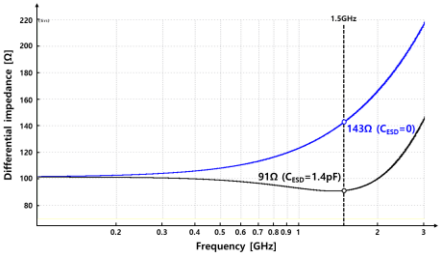


Fig. 11 Differential impedance plots in case of without and with parasitic capacitance of ESD protection circuit.

the ESD protection circuit, it will not need heavy efforts to reduce parasitic capacitance of ESD protection circuit. If we let the parasitic inductance of COF package be L_{COF}, total amount of the parasitic capacitance of clamp diodes be C_{ESD}, and half of the on-die termination resistor as R_{TERM}, simplified equivalent half-circuit including COF package trace, parasitic capacitance of ESD protection circuit, and on-die termination resistor can be illustrated as Fig. 12. The input impedance of the circuit can be calculated as Eq. (1). It is impossible to find frequency-independent fixed L_{COF} and C_{ESD} values. Therefore, when sweeping the capacitance values from 0pF to 2pF as Eq. (2), 1.4pF is derived as the capacitance value which has minimum standard deviation from the target impedance 100Ω over the frequency range of interest from 100MHz to 2.7GHz, up to 2nd harmonic of the center frequency.

$$Z_{in} = \frac{R_{TERM}}{1+\omega^2 {R_{TERM}}^2 {C_{ESD}}^2} - j\omega\left(\frac{{R_{TERM}}^2 C_{ESD}}{1+\omega^2 {R_{TERM}}^2 {C_{ESD}}^2} - L_{COF}\right) \quad (1)$$

$$\sigma = \sqrt{\frac{1}{n}\sum_{n}\left(\mu - Z_{in,n}\right)^2} \quad (2)$$

where, μ = target impedance = 100Ω

Fig. 13 shows the simulated eye opening diagram when C_{ESD} values are 0pF and 1.4pF, respectively. It is assumed that the data rate is 2.7Gbps, test point is the nearest S-IC input stage from FFC connector with 500mm length of FFC, and no equalizer options are applied. Wide eye opening in both eye height and width was obtained when C_{ESD} is 1.4pF. Based on this result, it was demonstrated to achieve better eye opening at a receiver side by optimizing

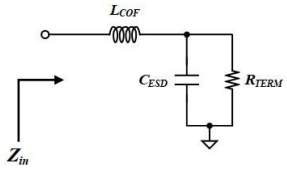
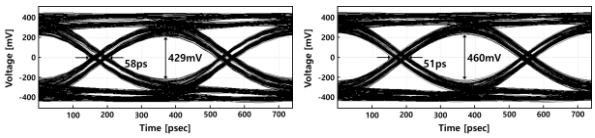


Fig. 12 Simplified equivalent half circuit for impedance calculation.



(a) (b)

Fig. 13 Simulated eye opening diagram when (a) C_{ESD}=0pF and (b) C_{ESD}=1.4pF.

the high-speed input signal trace design on COF package under the given parasitic capacitance of ESD protection circuit, or optimizing the on-chip capacitance including parasitic capacitance by ESD protection circuit under given parasitic inductance of COF package trace.

3 Conclusions

This paper reviewed FPC cable, FFC, and COF designs in terms of impedance matching and crosstalk, and their design guides are presented. Even if the FPC cable is so short, if it is not designed to reduce crosstalk noise, it could be a bottleneck of determining the final quality of the signal. In case a long FFC is needed, its insertion loss has to be significantly considered as well as impedance matching so as not to degrade the overall signal quality of the system. Finally, if parasitic capacitance of on-chip ESD protection circuit is designed to compensate parasitic inductance of COF package trace, better eye opening can be obtained. Designing flexible channels considering impedance matching and crosstalk reduction brings better SI performance in high-speed intra-panel interface system in 8K TV applications.

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