

High Resolution Array Tester for Flat Panel Display Using Proximity Capacitance Image Sensor

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ABSTRACT

An array tester technology using a proximity capacitance image sensor with high resolution and high-speed performance identifying electrically positions and types of defects on flat panel substrates are discussed. Some results of defects on lines and pixel-electrodes on LCD and Mini-LED panels using the array tester are demonstrated.

1 Introduction

In recent years, there is an increasing demand for identifying defect positions on array substrates in the manufacture of high-resolution smartphone panels to improve yield. In the conventional defect inspection, an optical inspection using a microscope is performed after an electrical inspection using a pin prober jig [1,2] to identify the position. In contrast, the high-precision, real-time capacity detection method using independently developed proximity capacitance image sensor [3,4] easily identify the Open/Short defect position of a high-resolution smartphone with few false detections. Defects on transparent electrodes (ITO electrodes), metal bump heights, and via hole depths are also detectable with the sensor. Internal wirings are observed even if the surface is covered with opaque resin. Periodic pattern inspection that tends to cause interference fringes is possible. In addition, this inspection causes no damage on the board under test and requires no jig for each type of the board under test. The coordinates of the defect position specified on the image, are easily linked to the repair system. Potential defects such as fatness, thinness, chipping, dents, and misalignment are also detected.

In this paper, the operating principle of the proximity capacitance image sensor, and the defect detection results on the substrate of LCD and Mini-LED displays, and reduction of inspection time with tiled sensors are presented.

2 Proximity capacity imaging

2.1 Proximity capacitance image sensor

As shown in Fig. 1(a), our novel sensor consists of tiny floating detection electrodes which are two dimensionally arrayed and coupled with ground with the capacitance

(C_c). When a conductive target such as metal circuitry on array substrate of FPD approaches to this detection electrode, the target itself works as a reference electrode and capacitance between the target and each detection electrode (C_s) can be measured in the method in Fig. 1(b). Consequently, the two-dimensional capacitance distribution is obtained along the target.

This sensor has two parallel signal outputs for V_{OUTN} and V_{OUTS} . Here, V_{OUTN} and V_{OUTS} are the reference and signal voltage levels, respectively. Both V_{OUTN} and V_{OUTS} contain same the kTC noise and the fixed pattern noise (FPN). By taking difference between V_{OUTN} and V_{OUTS} , the kTC noise and FPN are cancelled out, and the signal voltage V_{OUT} expressed by the following equation (1) is obtained.

$$V_{OUT} = V_{OUTN} - V_{OUTS} = \frac{C_s}{C_c + C_s} \cdot V_{IN} \cdot G \quad (1)$$

Here, V_{IN} shows the input voltage to the target, G shows the readout gain from the detection electrode to the output amplifier in the image sensor.

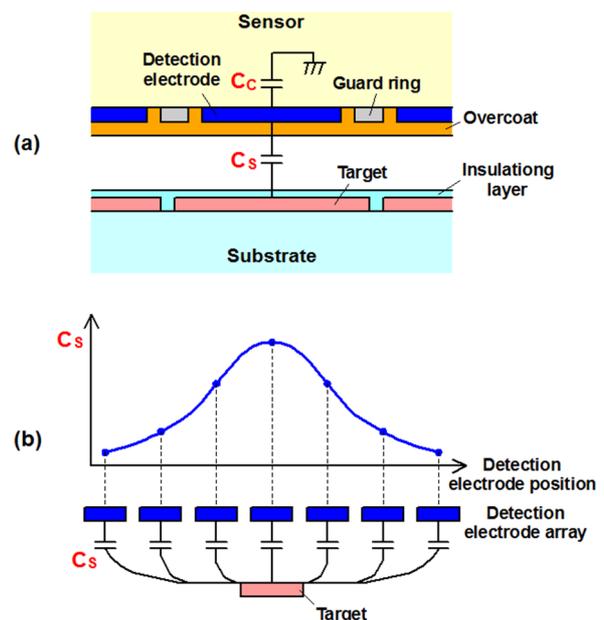


Fig. 1 Measurement configurations

By this advanced noise cancelling operation, high capacitance detection accuracy is obtained.

Table.1 shows the characteristics of the sensors in production, planned release, and under development.

In this experiment, a 12 μm pixel product that was mass-produced in 2020 was used. For all sensors, the noise reduction technology described above has enabled to achieve highly accurate capacitance detection in a range of 0.1 aF.

In addition, the developed proximity capacitance image sensor system was named “EPIS” (Electrical Picture Inspection System).

2.2 Flat panel testing method

Fig. 2 shows an image of a flat panel display with an Open defect when a signal is applied to the metal wires and inspected by EPIS. Since the C_s becomes large and appears white in the portion where the signal is reached, whereas the C_s becomes small and appears black in the portion where the signal is not reached, hence, defects are visualized.

In addition, if a sensor with a pixel size of $5.6 \mu\text{m} \times 5.6 \mu\text{m}$ is used, flat panels up to 750 ppi can be inspected according to the sampling theorem.

However, since the flat panel display must be inspected with non-contact, the C_s becomes small and the V_{OUT} also becomes small. Therefore, low noise performance that enables high-precision detection on the order of aF is indispensable.

Table. 1 Capacitance image sensor products

	2020 Product	2021 Release	2021 Development
Technology	0.18 μm 1P5M CMOS		
Pixel area [mm \times mm]	12.96 ^H \times 12.96 ^V	12.9 ^H \times 12.9 ^V	3.94 ^H \times 3.58 ^V
Number of pixels	1,080 ^H \times 1,080 ^V	2,304 ^H \times 2,304 ^V	1,408 ^H \times 1,280 ^V
Pixel size [$\mu\text{m}\times\mu\text{m}$]	12 ^H \times 12 ^V	5.6 ^H \times 5.6 ^V	2.8 ^H \times 2.8 ^V
Sampling frequency [MHz]	20	20	>20
Frame rate [fps]	11	8	>8
Detection accuracy [aF]	0.1		

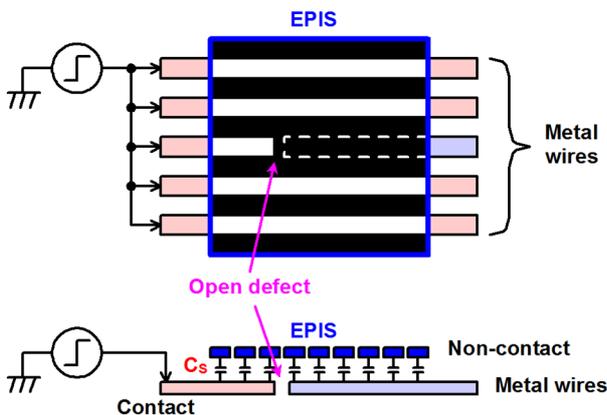


Fig. 2 Flat panel testing method

2.3 Experimental equipment

Fig. 3 shows the experimental equipment of the capacitance image sensor.

The sensor head with a 12 μm square pixel sensor chip in the center is mounted on a guide that moves horizontally. The sensor surface fixed downward moves step-and-repeat method along the horizontal direction while maintaining a space gap of 40 μm between sensor surface and the target substrate, so that the entire large panel substrate is inspected. The spatial resolution of the sensor is about 20 μm , which is about a half of the spatial gap. The scanning speed of the sensor head is 0.8 second per step. In the following experiment, the voltage V_{IN} applied to the target substrate is 25 V.

3 Results & Discussion

3.1 Inspection of FPD

Fig. 4 shows an inspection result of a liquid crystal display. Optical inspections cannot detect the potential on charged transparent electrodes or pixels, however, capacitance inspection clearly shows the defects. In this example, a line defect in the column direction tells a situation in which the pixels in said column were not charged with a signal. In addition, it also detects point defects in the same basis.

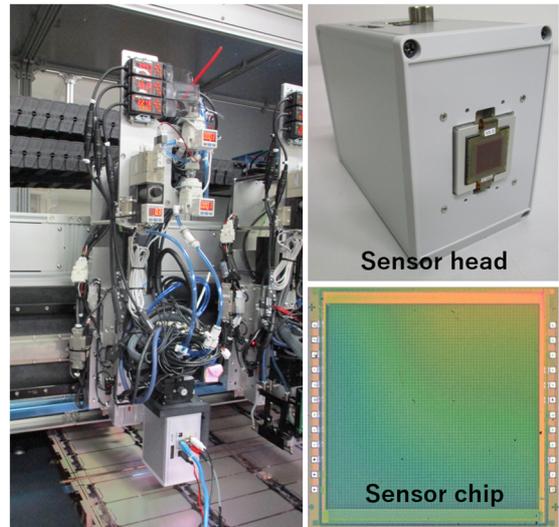


Fig. 3 Experimental equipment

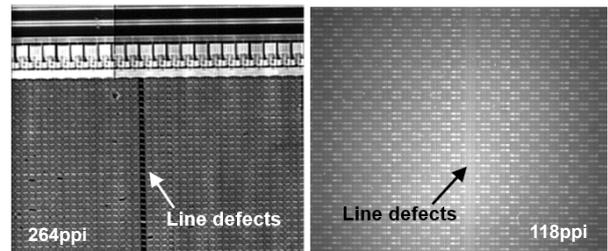


Fig. 4 Capacity inspection of the potential charged in the LCD pixel

Fig. 5 shows a comparison of the detected images of existing VIOS (Voltage Imaging Optical System) [5] and EPIS. Similar to EPIS, VIOS has the ability to locate defects which cannot be detected by optical methods without contact. EPIS was clearly superior in terms of spatial resolution and image contrast ratio. Furthermore, VIOS, which has limited spatial resolution, cannot inspect modern smartphone panels above 500 ppi, but EPIS with a pixel size of $5.6 \mu\text{m}$ and smaller air-gap can inspect them.

Fig. 6 shows EPIS images of various defects on the LCD array substrate. The EPIS image clearly identified the defect position and type with high defect detection rate.

Mini-LED substrates for simple color displays can also be inspected by EPIS. The substrate consists of numerous pads for LEDs on one side connected through multi rewiring layers with the output of driver ICs on the other side. Fig. 7 depicts the cross-section of the substrate schematically. Typical substrate having 180×120 pixels has more than 80,000 pads on the surface, therefore it is unrealistic to contact probe pin on each pad.

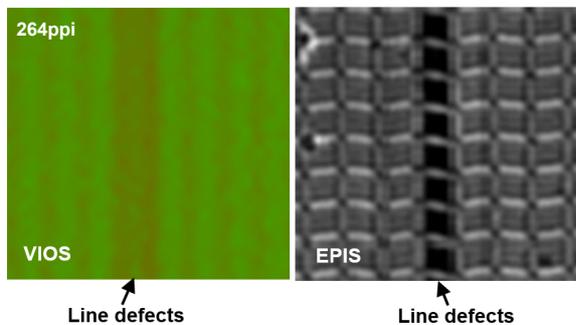


Fig. 5 Comparison of detected images of VIOS vs EPIS

Defect type	EPIS image	EPIS Enlarged image
Gate & Data Short	85ppi 	
Data Open	85ppi 	
ITO Open	85ppi 	

Fig. 6 LCD defect detection images

In order to obtain EPIS data on LED pads, inspection voltage pulses are applied through the pins attached to the pads connected through rewiring layers to the corresponding groups of LED pads such as R, G, B, Data. By comparing with OK samples data, defective pads were clearly observed as shown in Fig. 8.

Touch sensors, as important components of the display, were also inspected. Identifying the defect position in trace wiring is crucial to avoid continuous NG production. Recent trends of finer L/S make more difficult to specify the position of defects, however, EPIS was proved to contribute to prompt identification of such defect positions.

3.2 Reduction of inspection time with tiled sensors

Since the current pixel area shown in Table 1 is so small that the number of the steps in the step-and-repeat method becomes numerous for inspecting entire LCD and AMOLED array substrates, causing unfavorable long inspection tact time. One of the solutions we considered is to increase the detection area. However, the sensor itself is manufactured in a CMOS process, so there is a limit in size of the pixel area of the sensor, due to the limitations of the manufacturing equipment and the yield rate. Therefore, tiling multiple sensor chips is chosen to reduce the inspection tact time.

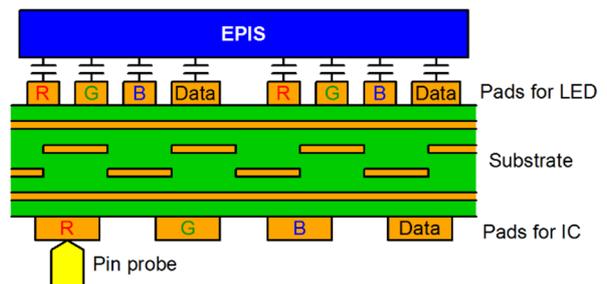


Fig.7 The schematic cross-section of Mini-LED substrate

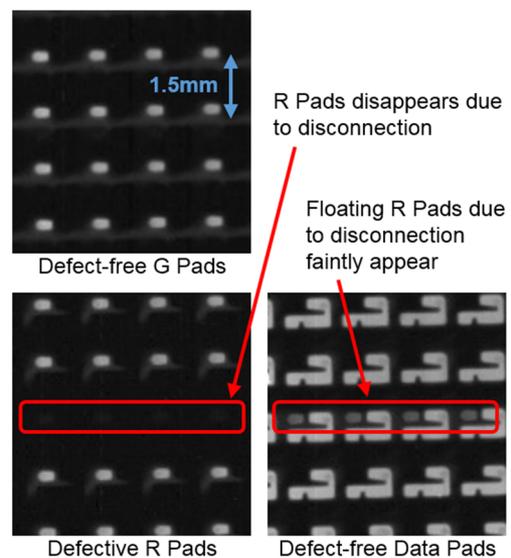


Fig.8 EPIS images of defective Mini-LED substrate

As shown in Fig. 9, about 20 mm x 20 mm size sensor chips, which is suitable to be realized by a general exposure machine, were tiled in 2 x 4 with separations equivalent to the chip size of a sensor. The tiled sensors can inspect smartphones of two different size in four steps per cell as depicted in Fig. 9. By using these tiled sensors, the inspection tact time for the 6th generation panel will be nominally reduced to about 1/7 compared to the case of a single sensor chip. Furthermore, the inspection tact can be even more shortened by increasing the number of inspection heads in the tiled sensors.

As a significant point, if there is a variation in the height of each tiled sensor chip, the capacitance will change, which will greatly affect the output image. Therefore, in order to achieve high-precision flatness, while keeping sensor chips steadily pressed on surface plate, these multiple chips were bonded with the substrate at the same time.

4 Conclusions

The defect detection and verification results for LCD and Mini-LED array substrates using the originally developed proximity capacitance image sensor were presented. Currently, a high-precision array tester which utilizes such sensors is being developed. By combining defect position detection and high-definition, high-contrast ratio visualization image data with a repair device, the efficiency of inspection and repair shall be significantly improved. Furthermore, by improving the panel yield at the array substrate stage, the effect on reducing the panel manufacturing cost is also significant. In particular, the latest AMOLED panels for smartphones have a resolution of 500 ppi or higher, many elements in the pixel circuit, and fine wiring patterns, and then it is desirable to inspect with higher resolution sensors such as EPIS. The finer circuitry will be, the better resolution sensors become important. EPIS is expected to be widely used in various fields in a non-destructive and non-contact technology where conventional optical inspections are incapable.

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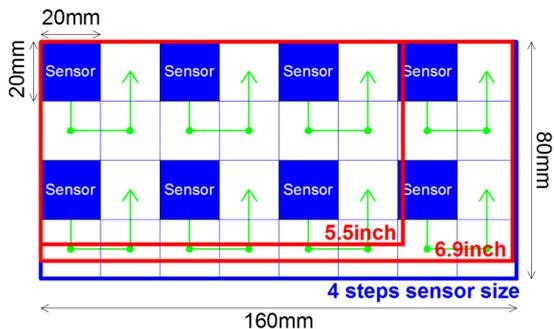


Fig. 9 Sensor tiling arrangement and smartphone panel size