

Cu Process Development in 50UD 120Hz LCD TVs Integrated GOA Gate Driver Circuit using Halftone Photolithography Four-Mask a-Si TFT Architecture Technology

An-thung Cho, Wen-Bing Wu, Hao Dong, Yao-Feng Tsai, Yong Zhang, James Hsu, Wade Chen

E-mail address: david.cho@szhk.com.cn

ChuZhou HKC Optoelectronics technology Co., Ltd., China

Keywords: 50UD 120Hz LCD TVs ; Four-Mask a-Si TFT ; Cu Process

ABSTRACT

A mechanism of high doped N+ film was used to lower the contact resistance between metal and semiconductor to achieve ohmic contact in 4-mask process. In this article, the improvement mechanism to reduce contact resistance by using high doped N+ layer will be investigated in conjunction with energy level diagram.

1 Introduction

The copper process mainly uses copper wires to replace existing aluminum wires as scan lines and data lines, as shown in Fig.1. When using copper wires, it can reduce the resistivity of the signal line, introduce high-frequency drive technology, design large-tolerance circuits, reduce the number of ICs, and reduce costs; it is conducive to narrow bezels, increasing aperture ratio, improving image quality, energy saving and environmental protection, and meeting Large size, high resolution and high refresh rate, high functionality. Now, enhancing the production yield rate are critical for the mass production. A-Si:H TFT manufactured by using four-mask process instead of normal five-mask process to improve the low manufacturing cost and high yield rate is a good solution, the four-mask technology is used to reduce a photolithography steps, the two-Wet and two-Dry(2W2D) technology is adopted.

Because copper has the characteristics of corrosion and oxidation, it is very challenging in production. At present, most panel factories use copper acid with fluoride and high H₂O₂ to etch Cu. But this method will be harmful to human body and machine. After repeated trials and optimization of the process, we use fluorine-free and low H₂O₂ cupric acid and successfully imported it into Mo/Cu structure TFT-LCD, as show in Fig.2. Etching without F cupric acid can also achieve the effect of F cupric acid, and M1 the average taper angle is 42 degrees, M2 the average taper angle is 46 degrees, as show in Fig. 3. Fig. 3(a) is a cross-sectional view of M1 etching, and Fig. 3(b) is a cross-sectional view of M2 etching

The Cu process has many advantages compared to the Al process, but in the Cu process TFT, the contact resistance between the metal and the semiconductor is larger, which will lead to insufficient charging rate of the

TFT. We discuss its mechanism in detail and give improvement measures.

2 Results

2.1 Comparison of electrical properties between Cu process and Al process

Fig.4 (a) shows the IdVd diagram of Cu process and Al process when V_g=10V, it can be seen that under the same V_d voltage, the current I of Al process is much larger than that of Cu process. $K=(I_d-I_0)/(V_d-V_0)$, the slope K is expressed as the reciprocal of resistance, which is the conductivity σ . The electrical conductivity of Al process TFT is much greater than that of Cu process as shown in Fig.4 (b). Table 1 is obtained by calculation. When V_d=5V, the conductivity of Al process is 100%, Cu process is only 60%. When V_d=30V, the conductivity of Al process is 50.3%. Cu process is only 14.6%. In order to more clearly analyze the reason why the conductivity of Cu process is much lower than that of Al process, a detailed explanation is given below through the band diagram.

2.2 Metal and n-Si contact energy level diagram

The current generated by the MIS structure in the TFT device must be input and output from the source and drain. The impedance between the MIS structure and the external signal line is expected to be a low resistance state, which is through the MS structure ohmic contact between the n-Si and the source and drain to realize. The ohmic contact resistance is inversely proportional to the P doping concentration in n-Si and directly proportional to the metal work function. Assuming that metal and n-Si have a common vacuum electron energy level, and the work function of the metal is greater than that of n-Si, $W_m > W_s$. Before they contact, the energy level diagram before reaching equilibrium is shown in Figure 5(a). Obviously, the Fermi level (EF)_S of n-Si is higher than the Fermi level (EF)_m of metal, and $(EF)_S - (EF)_m = W_m - W_s$. When metals come into contact with n-Si, they become a unified electronic system. $W_m > W_s$, a positive space charge zone is formed on the semiconductor surface, in which the electric field direction is directed from the body to the surface, which

makes the electron power of the semiconductor surface higher than that of the body, and the energy band is bent upward to form a surface barrier. In the barrier region, the space charge is mainly formed by ionized donors, and the electron concentration is much smaller than that in the body, so it is a high resistance region, often called a barrier layer. As shown in Figure 5(b). The barrier height for electrons flowing from metal to a-Si is ϕ_{b0} , is the work function of the metal, and χ is the electron affinity of n-Si. Under the same n-Si conditions, the work function of MoN(4.18eV) is smaller than Mo (4.6eV), so the barrier height in the Bottom-Mo/Cu structure is greater than that of Bottom-MoN/Al structure, making Cu and n-Si contact resistance is relatively large, resulting in poor conductivity[5]. By increasing the P doping concentration in n-Si to form the energy band diagram shown in Figure 5(c), the carriers can tunnel through instead of crossing the barrier, and the contact resistance is small. Therefore, in order to improve the conductivity of the Cu process, doping high concentration P in the n-Si layer in contact with the metal is an effective method. In addition, using low-speed film formation on n-Si in contact with the metal to improve the surface state of n-Si may also be an effective method. We will do further verification tests next.

2.3 Cu Process TFT-LCD Fabrication

Fig.6 shows the display images of the 50 inch UHD 120Hz TFT-LCD panel with Cu process using 4-mask a-Si TFT which was fabricated on HKC display's G8.6 (H2) LCD line.

3 Conclusions

In order to solve the problem of G picture difference caused by insufficient Ion in Cu process TFT-LCD. Comparative of the electrical characteristics of the Cu process and the Al process, the conductivity of Cu process is less than that of Al process. And analyze this reason in detail through the metal-semiconductor contact energy level diagram. Provide feasible measures to solve the problem of Cu process TFT-LCD.

Acknowledgements

This section provides instructions for submission of your technical summary manuscript

References

- [1] Kim, Da Eun, et al. "Corrosion Behavior and Metallization of Cu-Based Electrodes Using MoNi Alloy and Multilayer Structure for Back-Channel-Etched Oxide Thin-Film Transistor Circuit Integration." IEEE Transactions on Electron Devices 64.2(2017):447-454.
- [2] Yeon, Han Wool, et al. "Cu Diffusion – Driven Dynamic Modulation of the Electrical Properties of Amorphous Oxide Semiconductors." Advanced Functional Materials 27.25(2017):1700336.
- [3] Cheng Wei Lin, Mo Hsun Tsai. "Etchant compositions

and etching method for metals Cu/Mo." US patent No. 2010/0301010 A1.

- [4] Bo-Hyun Seo, Jae-Hong Jeon, Jorg Winkler et al. "A study on the galvanic reaction between Cu and Mo as well as MoW for TFT-LCD by using a zero-resistance ammeter." SID09 Digest, 1320-1323.
- [5] Lin R L, Lu Q, Ranade P, et al. "An adjustable work function technology using Mo gate for CMOS devices." Electron Device Letters IEEE, 2002,23(1):49-51.
- [6] Y.H. Jang, "Instability of Shift Register Circuits Using Hydrogenated Amorphous Si TFTs", Jap. J. Appl. Phys. 45, pp. 6806-6811, 2006.
- [7] W.B. Jackson, J.M. Marshall, M.D. Moyer, "Role of Hydrogen in the Formation of Metastable Defects in Hydrogenated Amorphous Silicon", Phys. Rev. B.39, p.1164, 1989.
- [8] H. Lebrun, N. Szydlo, E. Bidal, "Threshold-voltage Drift of Amorphous Silicon TFTs in Integrated Drivers for Active Matrix LCDs", J. of the SID 11/3, p.539, 2003.
- [9] S. F. Chen, L. H. Chang, J. R. Chen, S. C. Lin et al, "Integrated a-Si TFT Gate Driver with Reducing Clock Duty Ratio," SID Symposium Digest of Technical Papers, 2009, p.1092-1095.
- [10] Y.H. Jang, S.Y. Yoon, B. Kim, M. Chun, H.N. Cho, S. C. Choi, N.W. Cho, S.H. Jo, K.-s. Park, T. Moon, C.-D. Kim and I.-J. Chung, "a-Si TFT Integrated Gate Driver with AC driven Single Pull-down Structure", SID Digest, pp.208-211, 2006.

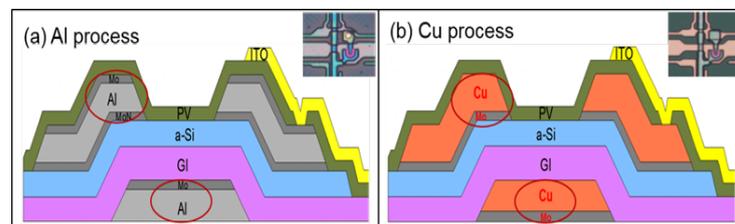


Fig. 1 (a) Cu-Cu 4 Mask structure diagram (b) AL-Al 4 Mask structure diagram

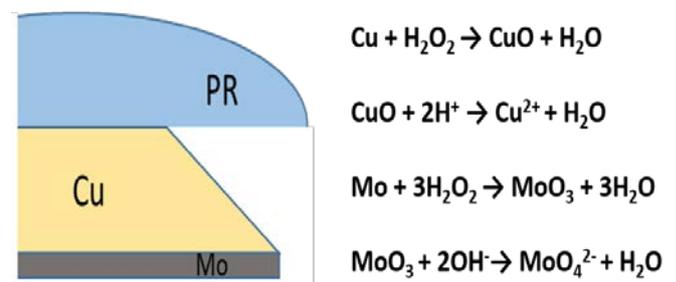


Fig.2 Acid etching Cu principle

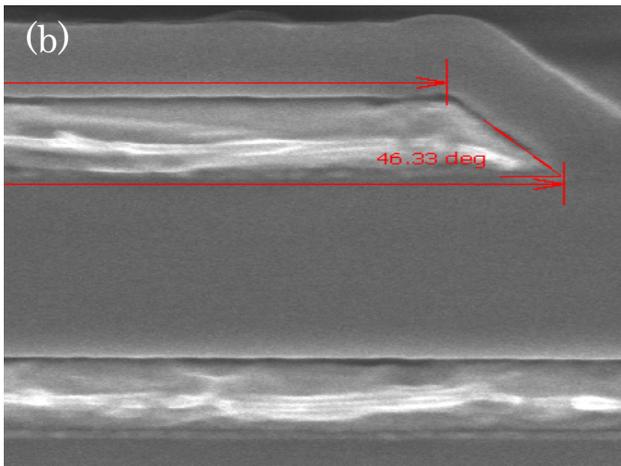
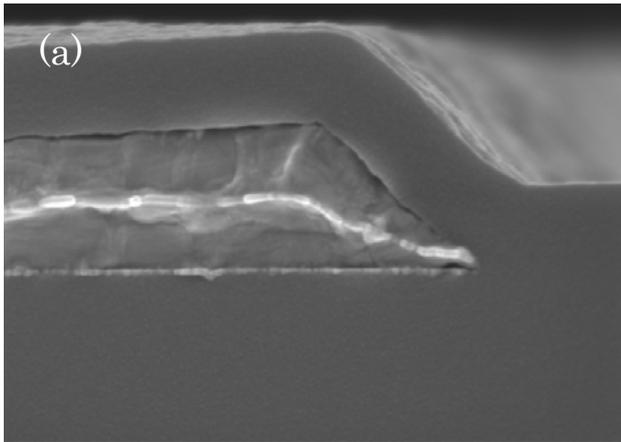


Fig. 3 (a) M1 SEM cross-section image after copper acid etching (b) M2 SEM cross-section image after copper acid etching

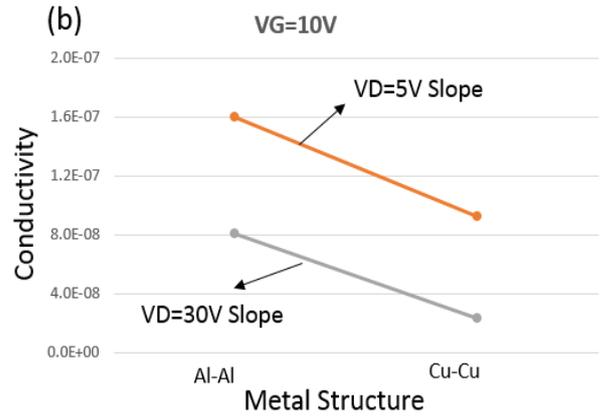
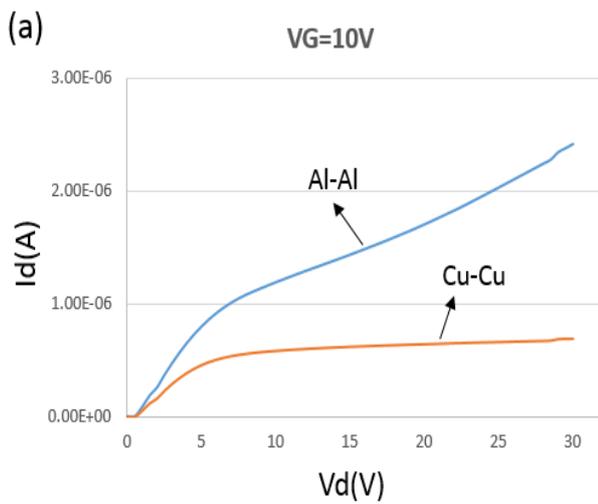


Fig. 4 (a) the IdVd diagram of Cu process and Al process (b) the slope diagram of Cu process and Al process at Vd=5V and Vd=30V

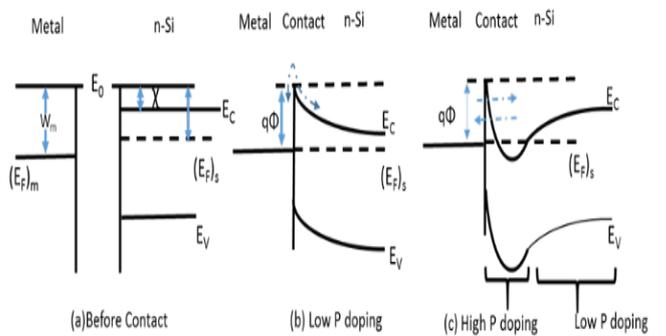


Fig. 5 Metal and n-Si contact energy level diagram



Fig. 6 50 inch UHD 120Hz TFT-LCD panel with the Cu process using 4-mask a-Si TFT

Table 1 Cu-Cu Al-AI conductivity percentage

Voltage	σ_{Al-AI}	Percent	σ_{Cu-Cu}	Percent
VD=5V	1.60E-07	100%	9.25E-08	60%
VD=30V	8.03E-08	50.3%	2.32E-08	14.6%