The Early Work on Sputtering Formation of Amorphous IGZO (In-Ga-Zn-O) Channel and SnO Channel TFTs

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Keywords: IGZO (In-Ga-Zn-O), sputtering, thin-film transistor (TFT), amorphous, oxide semiconductor.

ABSTRACT

We introduce our research activities of sputter-fabricated amorphous In-Ga-Zn-O (IGZO) TFTs, which we firstly achieved more than 10 years ago. We proved that uniform fabrication of high-performance a-IGZO TFTs was easily achieved by sputtering. Investigations of sputter-formed p-type SnO TFTs we made are also mentioned.

1 Introduction

In 2004, the first demonstration of amorphous oxide semiconductor (AOS) thin film transistor (TFT) using amorphous In-Ga-Zn-O (*a*-IGZO) channel layer fabricated at room temperature was reported by Hosono's group (Tokyo Institute of Technology), which showed excellent characteristics in comparison to hydrogenated amorphous silicon (*a*-Si:H) TFTs, e.g., field-effect mobility (μ_{FE}) of 7 $cm^2V^{-1}s^{-1}$, approximately one order of magnitude larger than *a*-Si TFTs [1]. Substantially, our research group started joint research with Hosono's group to put the AOS TFT technology into practical use.

Our objective was to fabricate AOS TFTs uniformly on large area, because the first *a*-IGZO TFT was fabricated by pulsed-laser deposition (PLD) method, which can form oxide thin films so softly enough to keep the interface between *a*-IGZO channel layer and gate insulator clean, but only on small area. For this objective, we chose **sputtering** method to deposit this oxide semiconductor channel layer uniformly on large area, because large area film-deposition by sputtering had been implemented for transparent oxide conductor films such as indium tin oxide (ITO) electrode films and it seemed difficult to develop a deposition process for such oxide films using softly forming method like evaporation, chemical vapor deposition (CVD), etc.

This challenge seemed lacking in common sense at that time because the surface of the deposited film was bombarded with high-energy argon, oxygen and metal ions generated in a sputtering plasma atmosphere, and this bombardment damaged the channel-insulator interface with creation of trap-sites. Therefore, this was so ambitious attempt that most of experts in TFT fabrication thought it impossible to realize. However, we believed that such oxide semiconductors with metal-oxygen ionic bonds created such traps adversely affecting channel operations not so easily by ion bombardment, compared to conventional semiconductor materials with covalency like silicon. Therefore, we started the study on sputtering formation of *a*-IGZO channel TFTs.

2 The first demonstration of *a*-IGZO TFTs by rf-magnetron sputtering [2]

Firstly, we used an old rf-magnetron sputtering machine used as a shared equipment in our laboratory. Deposition of both *a*-IGZO semiconductor and Y_2O_3 dielectric insulator films were carried out using this sputtering machine.

The problem we firstly found in the sputtering condition survey for forming *a*-IGZO channel layer was a control of oxygen content in the sputtering atmosphere. As shown in Fig. 1, electrical conductivity of *a*-IGZO film varied drastically from several $mS\cdot cm^{-1}$ to 1 $\mu S\cdot cm^{-1}$ (more than three orders of magnitude!) with slight increase of O_2 partial pressure from 16 to 20 mPa in total pressure of 0.53 Pa, equaling introducing O_2/Ar gas ratio of 3.1/96.9 to 3.7/96.3. This was too delicate to control because the same scale mass-flow controllers for Ar and O_2 were equipped to the sputtering machine for deposition of dielectric insulator films (e.g., O_2/Ar = 60/40 for Y_2O_3 deposition).

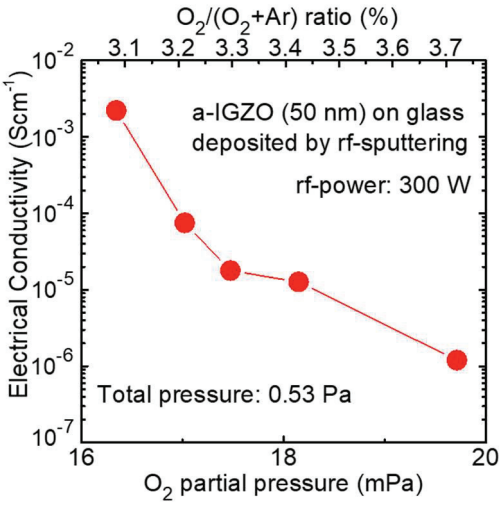

Fig. 1 Change in the electrical conductivity of the sputtered a-IGZO films as a function of O_2 partial pressure during sputtering. [2]

In order to solve this problem, we employed a diluted gas (5%-O_2 in Ar) connected to the third gas line in the sputtering machine. After that, electrical conductivity of sputter-deposited *a*-IGZO film became controllable and reproducible well.

The second problem for sputtering deposition was a chemical composition of *a*-IGZO. It is well-known that chemical composition of films deposited by sputtering usually deviates from that of alloy or compound targets due to difference of sputtering yield for each component element. Actually, chemical compositions of most *a*-IGZO films deposited by sputtering were In:Ga:Zn = 1:0.9:0.6, which was more largely deviated from the target composition (1:1:1) than the *a*-IGZO films by PLD (1.1:1.1:0.9) [1]. This would be a non-negligible character (phase separation would occur) if it were crystalline [3], but it is amorphous fortunately. Therefore, this composition deviation did not affect the overall performances (smoothness, uniformity, carrier mobility, etc.) for fabricating high-performance TFTs.

Next problem was substrate temperature raised by plasma exposure even no intentional substrate heating. A TFT structure for the first trial fabrication was a top-gate type with a stacking structure of Y_2O_3 insulator film (140 nm in thickness) on *a*-IGZO (50 nm) channel layer, as shown in Fig. 2 with deposition conditions for them. Sputtering durations were about 5 minutes for *a*-IGZO layer and 50 minutes for Y_2O_3 one. Surface temperatures rose to 40°C and 140°C after depositions of *a*-IGZO and Y_2O_3 layers, respectively. Even after Y_2O_3 deposition, it was confirmed that *a*-IGZO layer was still amorphous. Also we confirmed that this temperature rise after the sputtering process for Y_2O_3/*a*-IGZO deposition did not affect plastic substrates for flexible devices.

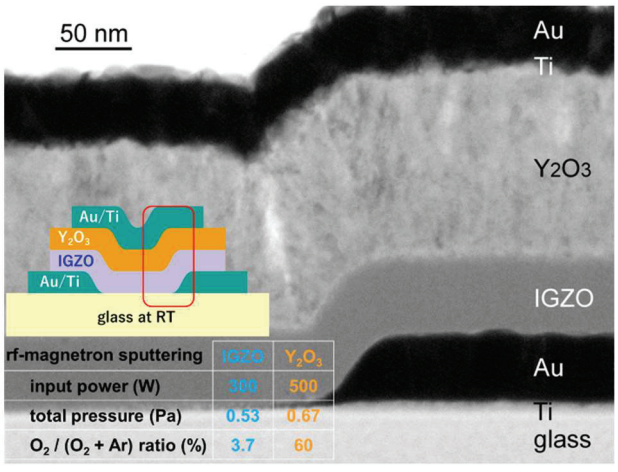

Fig. 2 Cross-sectional TEM image of the top-gate type a-IGZO TFT of which the channel (a-IGZO) and the insulator (Y_2O_3) layers were deposited by rf-sputtering. The inset shows a schematic of this TFT structure and deposition conditions of these a-IGZO and Y_2O_3 layers. [2]

After solving these problems, we successfully demonstrated the fabrication of a top-gate type *a*-IGZO channel TFTs with Y_2O_3 gate insulator on glass substrate by conventional sputtering process (Fig. 2). These TFTs with similar structure to the first demonstration fabricated by PLD showed characteristics (e.g., μ_{FE} = 12 $cm^2V^{-1}s^{-1}$, and on/off drain-current ratio of 10^8) almost the same as or better than those of the first one by PLD. Then, a lot of competitors entered the development of sputter-fabricated amorphous oxide channel TFTs.

3 Uniform fabrication of a-IGZO TFTs by rf-magnetron sputtering [4,5]

After this success, we employed another rf-magnetron sputtering machine only for study of oxide semiconductor TFTs. This machine was also for basic research with 3 targets of 3-inches in diameter. In order to improve uniformities of thickness, composition, electric properties, etc. of deposited films even using small targets, off-axis (target-substrate relation not face-to-face but diagonal) deposition was usually carried on.

Then we investigated uniform fabrication of *a*-IGZO TFTs (channel layer thickness of 20 nm) using thermal SiO_2 layer (100 nm in thickness) as a gate insulator of bottom-gate type TFT. Figure 3(a) indicates transfer characteristics and gate-leakage current properties of 96 *a*-IGZO TFTs with bottom-gate type structure (shown in the inset) fabricated in 1 × 1 cm^2 area. These TFTs show almost identical curves with good characteristics (e.g., μ_{FE} = 13 $cm^2V^{-1}s^{-1}$, and on/off drain-current ratio ≈ 10^{10}).

We then demonstrated uniform fabrication of bottom-gate type *a*-IGZO TFTs (channel layer thickness of 40 nm) with a sputter-deposited SiO_2 insulator film (200 nm in thickness) on a glass substrate. As seen in the TFT structure indicated in the inset of Fig. 3(b), not only SiO_2 films of good quality (insulating property, uniformity, smoothness, etc., which will be mentioned below) but also step-coverage (conformality) of the deposited films were required. Since the off-axis sputtering deposition geometry was also effective for improving step-coverage, probably due to diagonal incidence of sputtered particles onto the substrate, uniform and highly insulative films (no notable leakage at edges of bottom electrodes) were obtained. The fabricated 96 TFTs in 1 × 1 cm^2 area showed almost identical curves with similar characteristics (e.g., μ_{FE} = 10 $cm^2V^{-1}s^{-1}$, and on/off drain-current ratio ≈ 10^9) to those of the TFTs with thermal SiO_2 gate insulator layer (Fig. 3(a)), which insists that uniform fabrication of bottom-gate type *a*-IGZO TFTs using sputtering process was achieved even on glass substrate.

It was noteworthy that leakage current of the sputter-deposited SiO_2 gate insulator layer on bottom-electrodes with step-edges (Fig. 3(b)) was similarly low to the thermal SiO_2 (Fig. 3(a)), even taking difference of film-thicknesses into account. This may mean that we

achieved fabrication of high quality SiO_2 insulator films by sputtering. In our investigation, insulating property of SiO_2 film was independent of O_2 content in sputtering atmosphere; a highly insulative film could be obtained by sputtering even in 100% Ar atmosphere. Rather bombardment energy of Ar ions irradiated to the depositing film from the sputtering plasma might be dominant for controlling quality of SiO_2 film. Higher-energy Ar ion bombardment to film surface which was induced by higher rf-power or/and lower gas pressure resulted in not only increase of density of the film but also increase of Ar atoms implanted in the film, regardless of O_2/Ar content ratio in the sputtering gas. Therefore, insulating property of these SiO_2 films were highly correlated with Ar content in the film; leakage current decreases with increasing Ar/Si content ratio of sputter-deposited SiO_2 films as shown in Fig. 4. Interestingly, Ar impurity did not have harmful effect to the insulating property of SiO_2 films. Very thin layers of sputter-deposited SiO_2 films are adopted a part of gate insulator in some commercial products using *a*-IGZO TFTs.

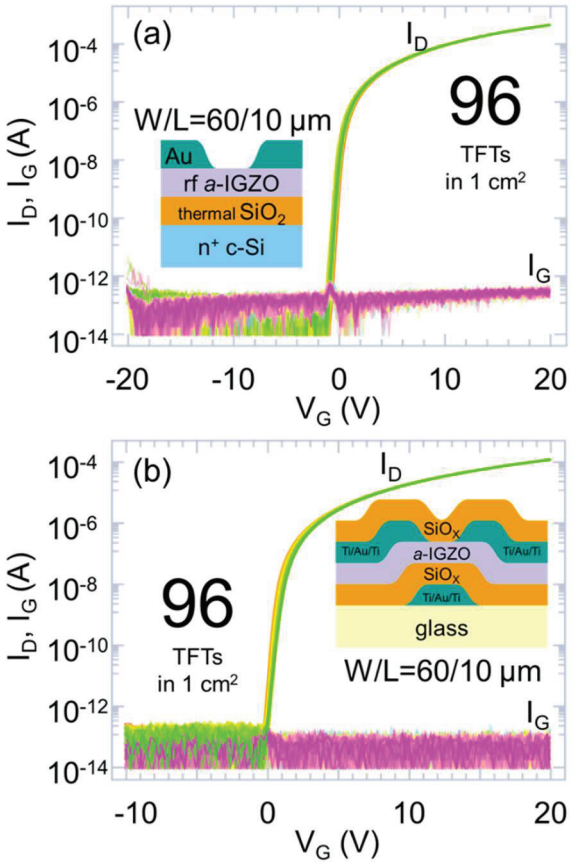

Fig. 3 Transfer characteristics and gate-leakage current property of 96 a-IGZO TFTs in 1 × 1 cm² area: (a) bottom-gate type TFTs with thermal SiO_2 gate insulator on Si substrate, (b) bottom-gate-type TFTs with sputter-deposited SiO_2 gate insulator layer (bottom) and protection layer (top of the TFT) on a glass substrate. [5]

For practical development of *a*-IGZO TFTs, the third sputtering machine with both dc and rf power sources and large-size targets (12.5 inches in diameter) was introduced. At that time, plasma-enhanced (PE) CVD was often employed to deposit SiO_2 and SiN_x insulator films, instead of rf-sputtering. PECVD-SiN_x films were also utilized for fabricating coplanar homojunction *a*-IGZO TFTs [7-9]. Investigation of *a*-IGZO TFTs was accelerated to more practical prototypes.

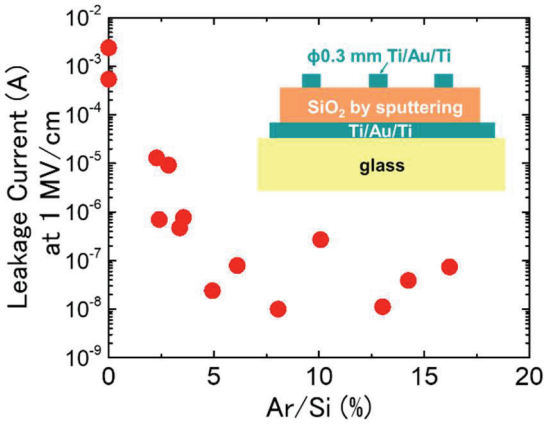

Fig. 4 Dependence of leakage current (at 1 MV/cm) on Ar/Si content ratio for SiO_2 films (about 200 nm in thickness) deposited by rf-sputtering. [6]

4 Sputtering formation of *p*-type SnO TFTs [10]

Among most of colleagues who aggressively pursued practical development of *a*-IGZO TFTs and devices with them, we started an investigation of *p*-type SnO TFTs by sputtering using the second rf-sputtering machine with small targets, just after Hosono's group reported *p*-type SnO TFTs epitaxially grown on single crystalline substrates by PLD with excellent characteristics in *p*-type oxide semiconductor channel TFTs, of which only several examples had been reported.

Since we confirmed that amorphous SnO did not work as *p*-type semiconductor, this investigation was firstly focused on how SnO was crystallized properly. The first trial was sputtering deposition on heated substrate with controlling sputtering atmosphere, but we did not obtain single-phase SnO films because of non-uniformity of substrate heating and plasma irradiation to depositing films. The second trial was post-annealing of amorphous SnO films deposited at room temperature by rf-sputtering for their solid-phase crystallization. In this attempt, a few of single-phase SnO films with *p*-type conduction were achieved, but the process window was very narrow; crystallization of SnO was very sensitive to not only annealing atmosphere and temperature but also sputtering condition for depositing amorphous SnO films.

Considering that the control of atmosphere in annealing process was insufficient (only gas flow control

in a tube furnace), we attempted to employ a capping layer on amorphous SnO for crystallization by annealing to prevent exposure to atmosphere. Conveniently, we possessed the technique to form high density, insulative, and chemically stable SiO_2 film at room temperature, as mentioned above. It was expected that this SiO_2 film shut off the atmosphere and only expelled a small amount of Ar gas by post-annealing process. Finally, single phase polycrystalline SnO films with *p*-type conduction were obtained stably by this attempt.

Then we fabricated SnO-TFTs with SiO_2 capping-layers by sputtering and post-annealing processes (Fig. 5(a)). After 300°C annealing, *p*-type TFT operation was successfully observed, and surprisingly a capped SnO-TFT after 400°C annealing showed an ambipolar (both *p*-type and *n*-type) behavior as shown in Fig. 5(b). Since it was confirmed that a SnO-TFT without capping layer was transformed to an *n*-type SnO_2-TFT by annealing in air, we proposed oxide semiconductor complementary transistor device (like "CMOS") structure using the *p*-type SnO and *n*-type SnO_2 channel layers formed selectively by the simple process (Fig, 5(c)).

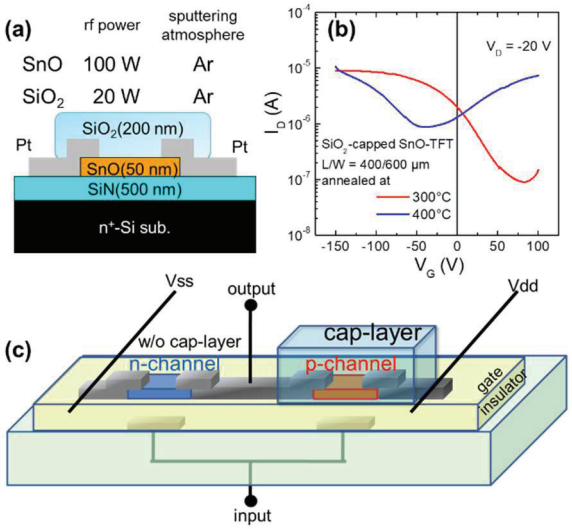

Fig. 5 (a) Schematic cross-section of polycrystalline SnO-TFT. (b) Transfer characteristics of SnO-TFTs with post-annealing at 300C and 400C. (c) A conceptual design of a SnO-based complimentary circuit. [10]

5 Summary

We introduced our investigations of *a*-IGZO and SnO channel TFTs using sputtering method, which were carried out more than 10 years ago. Fortunately, we firstly achieved *a*-IGZO TFTs fabricated by sputtering, then we proved that uniform formation of high-performance *a*-IGZO TFTs was easily achieved by sputtering. Also, we discovered ambipolar behavior of SnO-TFT and proposed an oxide CMOS structure based on SnO. We hope further development and spread of oxide semiconductors and devices with them formed by sputtering-processes.

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