InGaZnO Synaptic Thin-Film Transistor with AlOx Dielectric

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ABSTRACT

We demonstrate an InGaZnO (IGZO) synaptic thin-film transistor (TFT) fabricated by solution process. To mimic the electrical properties of biological synapses such as excitatory postsynaptic potential (EPSC), long-term potentiation (LTP), the AlO_x is used as a charge trapping layer of the IGZO TFT.

1 Introduction

Recently, in the era of AI and big data, the limitations of von Neumann architecture are emerging.[1] This is due to a bottleneck in systems where memory and processing are separated. Neuromorphic systems that can overcome these limitations by integrating memory and processing are attracting increasing attention.[2] Among the elements constituting the neuromorphic system, the role of the artificial synapse is the most important. This is because artificial synapses enable simultaneous process and have memory information.

There are many studies on 3-terminal synaptic transistors using metal oxide semiconductors such as IGZO[3], IZO[4], and InOx[5]. Metal oxide semiconductors are used in backplanes of display and sensors due to their excellent characteristics with low leakage and large bandgap.[6] To mimic the characteristics of biological synapses, they adopt materials such as AlOx, nanogranular SiO2 and HfZrOx for charge trapping, ionic electrolyte, and ferroelectricity as gate insulator (GI). Among them, aluminum oxide (AlOx) has good properties such as high breakdown field, large band gap, and relatively high dielectric constant.[7] In particular, it can be deposited by atomic layer deposition (ALD) and also by solution process. Recently, ferroelectric-like properties have been reported by charge trapping of aluminum oxide.[8]

2 Experiment

2.1 Fabrication of Device

The IGZO synaptic TFTs were fabricated on a Glass substrate with SiO_2 buffer layer deposited to prevent contamination. Mo was deposited by sputtering as a gate, source and drain electrode, and AlO_x was deposited by solution process as GI. For the semiconductor channel, IGZO was deposited by solution process, and SiO_2 deposited by plasma enhanced chemical vapor deposition (PECVD) was adopted for the passivation layer. The width and length of the fabricated TFTs are both 8 μm.

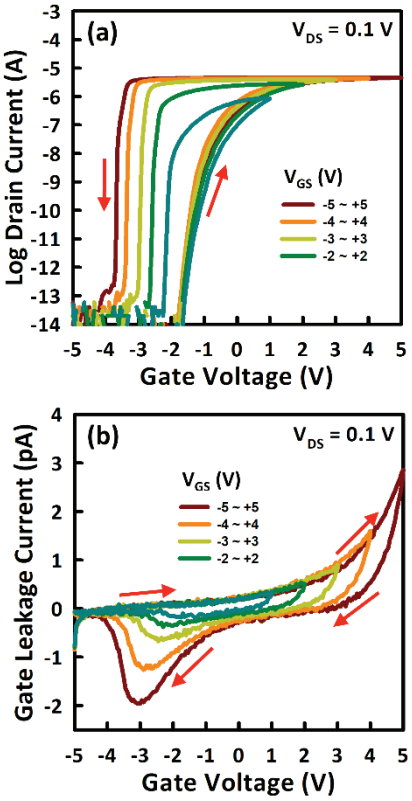

Fig. 1 Hysteresis characteristics of the synaptic IGZO TFT with AlO_x dielectric. (a) I_D and (b) I_G measured by sweeping V_G.

2.2 Electrical Measurements

All the electrical characteristics of the synaptic TFT were measured with a probe station at room temperature using a semiconductor parameter analyzer (Agilent 4156C). Presynaptic spikes were generated by pulse generator unit connected to an Agilent 51501B.

3 Results and Discussion

Figure 1 shows the hysteresis characteristics in transfer curve of IGZO synaptic TFT. In Figure 1a and 1b, the drain current (IDS) and gate leakage current (IG) measured while sweeping the gate voltage (VGS) were shown respectively. The VGS was first swept in the forward direction from -5 V and then returned to the opposite direction. We varied the maximum voltage in the range of voltage sweep from 2 to 5 V. In Figure 1a, a counterclockwise hysteresis characteristic is observed

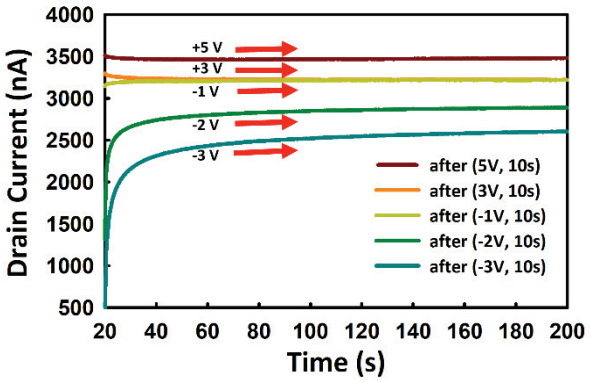

Fig. 2 Retention characteristics after applying 10s of Voltage pulse to gate. The voltage amplitude varied from -5 to +5 V.

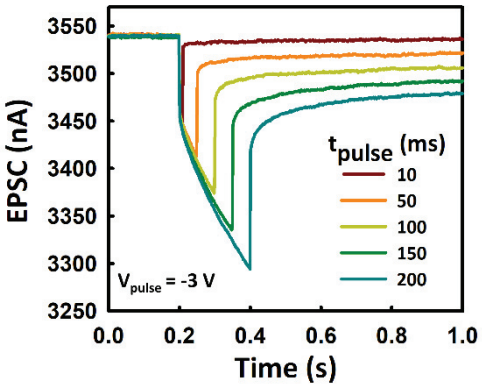

Fig. 3 Typical EPSC characteristics of the synaptic IGZO TFT.

for all gate voltage sweeps. It is confirmed that AlO_x has ferroelectric-like properties.[8] The hysteresis window, which is the change of threshold voltage (V_{th}) in the forward sweep and V_{th} in the backward sweep, is -0.95 V when the maximum voltage is 2 V and increases to -2.35 V when the maximum voltage is 5 V. There is a difference of 247%. This is because as the maximum voltage of the gate sweep voltage increases, more positive charges are trapped in the GI, which can be demonstrated through the I_G shown in Figure 1b. As the gate sweep voltage range is widened, the intensity of the peak in I_G while backward sweep due to the de-trapping of the trapped charges increases.[9]

Figure 2 shows the retention characteristics of I_{DS} according to the gate bias of the TFT. A 10 s of voltage pulse with the amplitude from -5 V to +5 V was applied to the gate and the change of I_{DS} for 180 s was measured. The results indicate that there is no significant change at -1 V, and at +3 V. But, when voltage amplitudes are -2 and -3 V, the current decreases to 359 and 644 nA after 180s compare with initial current before voltage pulse. Conversely, when the amplitude was +5 V, I_{DS} maintained an increase after 232 nA after 180 s retention. It can be explained that IGZO synaptic TFT has retention characteristics because trapped charge in the GI affects electrons in the IGZO channel.

Since the IGZO channel operates in depletion mode, it is more efficient to decrease the current by applying a negative voltage pulse than to increase the current by a positive voltage pulse. Therefore, negative voltage pulses were used for mimicking the electrical properties of biological synapses.

To mimic the properties of biological synapses functionally, a synaptic TFT corresponds to an element of a biological synapse as follows: The gate corresponds to pre-synapse, and voltage pulses relate to the presynaptic spike of a biological synapse applied. Since the source and drain correspond to the post- synapse, the drain current is recognized as the post synaptic current.

Figure 3 shows the characteristics of implementing excitatory postsynaptic current (EPSC), a basic characteristic of biological synapses. We measured EPSCs by applying a -3 V of voltage pulse to the gate with a pulse width of 10 to 200 ms. The I_{DS} decreases from 3.54 to 3.45 μA when a presynaptic spike of 10 ms is applied, and then increases to 3.53 μA after 500 ms. It can be explained the returning to the initial state after the pulse is applied. However, when the 50 ms of pulse is applied, it is 3.41 μA when pulse is over, which is 0.13 μA less than the initial current. And 500 ms after the pulse over, it is still about 15.5 nA lower than the initial state. Even when a 200 ms voltage pulse is applied, the difference of 42.9 nA remains compared to the initial state even after 500 ms. This is similar to the EPSC of biological synapses.[10] Through this characteristic, the synaptic behavior of IGZO TFT is confirmed.

Finally, long-term potentiation (LTP) characteristics are implemented shown in Figure 4. LTP enables learning and memory in biological systems.[11] To implement LTP in IGZO synaptic TFT, EPSC measured by applying 10 consecutive synaptic spikes is shown in Figure 5. The peak value of EPSC shows a tendency to increase linearly as the spike was applied. The initial EPSC value, which is 3,441 nA, decreases to 3,162 nA after the first spike, and decreases to 1,715 nA after the 10th spike. The △EPSC induced by the 10th spike is 618 % higher than the △EPSC induced by the first spike. From this result, we concluded that the IGZO synaptic TFT has the ability to learn because it remembers the information about the 10 spikes.

4 Conclusions

We demonstrate the solution processed IGZO synaptic TFT using AlO_x for GI that enable positive charge trapping. The mechanism that can modulate the channel conductance is analyzed through I_G of IGZO synaptic TFT. We conclude that the AlO_x layer deposited through the solution process at a low temperature of 275 °C allows the trap-assisted tunneling of electrons in the IGZO to the gate electrode. As a result, positive charge trapping occurs at the GI and semiconductor

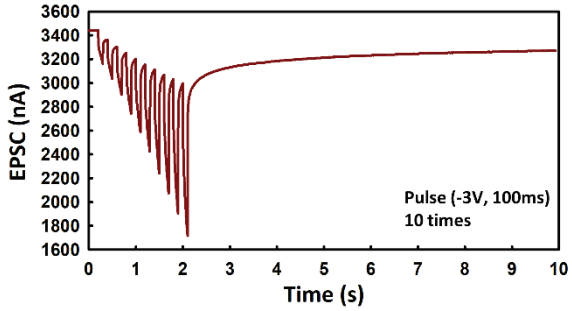

Fig. 4 LTP characteristics measured by applying 10 synaptic spikes.

interface. Finally, we demonstrate the device that electrically mimics the properties of biological synapses such as EPSC and LTP. Solution-processed IGZO and AlO_x layer has the advantage of low price and simple production process because of low temperature. Therefore, it will be a good candidate as an artificial synapse for future neuromorphic devices.

5 Acknowledgement

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References

[1] C. Mead, “Neuromorphic Electronic Systems,” Proceedings of the IEEE, vol. 78, no. 10, pp. 1629–1636, 1990, doi: 10.1109/5.58356.

[2] G. Indiveri and S. C. Liu, “Memory and Information Processing in Neuromorphic Systems,” Proceedings of the IEEE, vol. 103, no. 8. Institute of Electrical and Electronics Engineers Inc., pp. 1379–1397, Aug. 01, 2015. doi: 10.1109/JPROC.2015.2444094.

[3] M. K. Kim and J. S. Lee, “Ferroelectric Analog Synaptic Transistors,” Nano Letters, vol. 19, no. 3, pp. 2044–2050, Mar. 2019, doi: 10.1021/acs.nanolett.9b00180.

[4] C. J. Wan, L. Q. Zhu, J. M. Zhou, Y. Shi, and Q. Wan, “Inorganic proton conducting electrolyte coupled oxide-based dendritic transistors for synaptic electronics,” Nanoscale, vol. 6, no. 9, pp. 4491–4497, May 2014, doi: 10.1039/c3nr05882d.

[5] X. Liang, Z. Li, L. Liu, S. Chen, X. Wang, and Y. Pei, “Artificial synaptic transistor with solution processed InOx channel and AlOx solid electrolyte gate,” Applied Physics Letters, vol. 116, no. 1, Jan. 2020, doi: 10.1063/1.5120069.

[6] T. Matsuo, S. Mori, A. Ban, and A. Imaya, “Advantages of IGZO Oxide Semiconductor,” 2014.

[7] A. Daus et al., “Aluminum oxide as a dielectric and passivation layer for (flexible) metal-oxide and 2D semiconductor devices,” Mar. 2021, p. 49. doi: 10.1117/12.2587997.

[8] A. Daus et al., “Ferroelectric-Like Charge Trapping Thin-Film Transistors and Their Evaluation as Memories and Synaptic Devices,” Advanced Electronic Materials, vol. 3, no. 12, Dec. 2017, doi: 10.1002/aelm.201700309.

[9] A. Daus et al., “Positive charge trapping phenomenon in n-channel thin-film transistors with amorphous alumina gate insulators,” Journal of Applied Physics, vol. 120, no. 24, Dec. 2016, doi: 10.1063/1.4972475.

[10] R. S. Zucker and W. G. Regehr, “Short-term synaptic plasticity,” Annual Review of Physiology, vol. 64. pp. 355–405, 2002. doi: 10.1146/annurev.physiol.64.092501.114547.

[11] M. F. Bear and R. C. Malenka, “Synaptic plasticity: LTP and LTD,” 1994.