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1.5-inch, 3207-ppi OLED Display Enabled by Monolithic Integration of OSFETs and Si CMOS

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ABSTRACT

Oxide semiconductor field-effect transistors (OSFETs) can be stacked over silicon (Si) field-effect transistors (FETs). We used this technology to form Si–oxide semiconductor composite LSI and prototyped an OLED display in which Si FETs and OSFETs are monolithically stacked. This stacking enabled a larger screen and a lower power driver.

1 Introduction

Recently, xReality (XR), including augmented reality, virtual reality (VR), and mixed reality, has been attracting attention. Unlike smartphones, XR devices have a definition as high as thousands of ppi, requiring high luminance and a high frame rate. VR devices should also have a larger screen size. XR devices suffer from a screen-door effect when they have a low definition. Increasing the definition is an effective solution to this problem [1]. XR devices have disadvantageously low light usage efficiency due to their optical systems. Possible solutions for overcoming this are higher luminance and a larger screen size. However, increasing the screen size is limited by the shot size in the silicon (Si) substrate process, and combining a large screen size with high definition hinders high-frame-rate driving.

Generally, the mobility of bulk Si field-effect transistors (FETs) used in high-definition (HD) displays is too high in controlling the current of organic light-emitting diode (OLED) devices. Therefore, the channel length of Si FETs used as pixel FETs is long. It is difficult to lay out such long-channel-length FETs within a small pixel area, which is one problem facing HD displays formed using bulk Si FETs [2]. FETs formed using an oxide semiconductor (OS), which are referred to as OSFETs, do not need to have a channel length as long as that of bulk Si FETs and are suitable for HD displays. In fact, we have already demonstrated that an OLED display achieves a definition higher than 3000 ppi by including OSFETs [3,4].

The miniaturization of OSFETs has been proceeding in the field of large-scale integration (LSI) [5,6]. OSFETs have higher breakdown voltage than Si FETs [3,4], and are a promising technology enabling higher definition even when a more complex pixel circuit is employed. OSFETs have also been receiving attention as transistors that can be monolithically stacked over Si FETs. For example, memories and normally-off central processing units have been fabricated [7–10] by using the extremely low off leakage current of OSFETs [11]. Such devices are known as OSLSI.

Here, this OSLSI technology was used to develop a display. Specifically, source and scan drivers were formed using bulk Si FETs; then, pixels containing minute OSFETs were formed monolithically over the drivers [12,13]. In this manner, the shot size in the Si process was used to the maximum so that a screen size as large as 1.5 inches was achieved. Despite a 3840 × 2880 pixel count and a high definition of 3207 ppi, a high frame rate (120 Hz) and low power-consuming operation were possible because divided drivers can be arranged in this display. The OLED devices were formed by side-by-side patterning, allowing the OLED unit to have low power consumption and high luminance. Furthermore, the backplane of the display is mainly described below.

2 OLED/OS/Si Monolithic Structure and Characteristics of OSFET

Figure 1 shows a cross-sectional image of a structure in which OSFETs are stacked over Si complementary metal oxide semiconductor (CMOS).

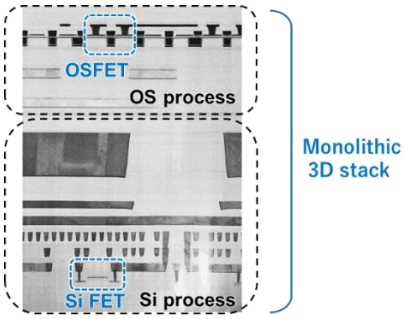

Fig. 1 Cross-sectional image

We employed this structure to develop an OLED display in which pixels were formed using OSFETs over the source and scan drivers that were formed using bulk Si FETs on a Si wafer. We call this display's structure an "OLED/OS/Si" monolithic structure, a concept view shown in Fig. 2. The drivers can be provided below the pixels in this structure, enabling the prototyping of a narrower-bezel display. Additionally, the shot area in the Si process can be used to the maximum, allowing for larger screen size.

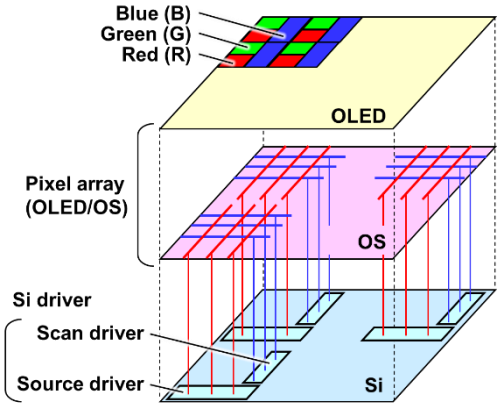

Fig. 2 Concept of OLED/OS/Si monolithic structure

Figure 3 shows a fabrication flowchart of the OLED/OS/Si display. First, Si FETs and wiring layers are formed over a Si wafer by a typical formation process of a driver IC. Subsequently, OSFETs and wiring layers are formed over the substrate. Then, the OLED unit is fabricated through evaporation and photolithographic patterning to complete a side-by-side OLED display. Since the Si FETs and the OSFETs are not bonded to each other but monolithically formed over one substrate, as earlier described, the Si drivers can be connected to the OS pixels arranged at a high density.

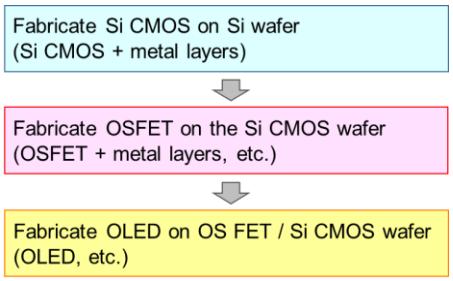

Fig. 3 Fabrication flowchart of OLED/OS/Si

Figure 4(A) shows the I_d–V_g characteristics of the OSFET. The graph shows that the OSFET has normally-off characteristics despite its ultra-small size (channel length (L): 200 nm, channel width (W): 130 nm, equivalent oxide thickness: 10.9 nm). The OSFET has a sufficiently low off-state current below the lower measurement limit of 1×10^{-12} A. Figure 4(B) shows the V_d breakdown voltage of the OSFET. The breakdown voltage is as high as approximately 20 V despite the ultra-small size; therefore, the OSFET is suitable for the backplane used for the pixel circuit of a display.

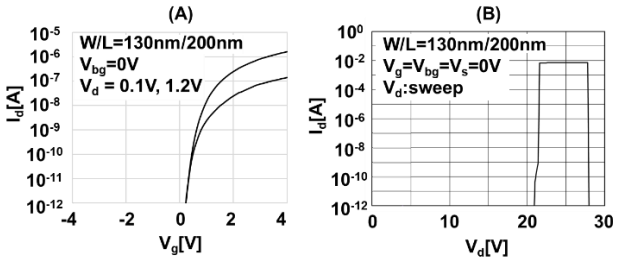

Fig. 4 Characteristics of OSFET

3 Driver Circuits

Increasing the screen size without compromising the high definition makes the number of pixels large. Therefore, this shortens one horizontal period, inhibiting high-speed driving at, for example, 120 Hz. Because of this, divided driver circuits were arranged in this prototype display, as shown in Fig. 5, which was enabled by the stacked-layer structure in which the drivers were formed using a Si layer, and the pixels were formed using an OS layer.

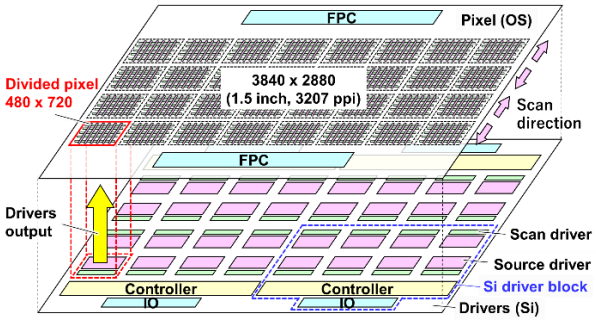

Fig. 5 Structure concept of the prototype display

In this OS/Si structure, the Si drivers: source and scan drivers, can be arranged in the entire display region. Therefore, they can be driven independently. Due to this characteristic of the Si drivers, 32 Si drivers were provided in the prototype display. Furthermore, the source and gate lines were divided into four and eight, respectively, to form 32 pixel arrays corresponding to the drivers. This division reduces the parasitic load of the source and gate lines and the number of devices causing a load during driving, which results in a reduced output load of the drivers. Additionally, the scan direction is controlled in each scan driver with an inter-integrated circuit (I^2C) interface such that gate lines of adjacent blocks are selected simultaneously.

Next, the structure of the Si driver circuit is described. The display with 3840 × 2880 pixels is driven with four Si driver blocks, making it 32 Si drivers. The primary components of each Si driver block are an input/output (IO) circuit, a low-voltage differential signaling (LVDS) circuit, a controller (I^2C module and a timing generator), and eight drivers: source and scan drivers. The LVDS circuit uses one clock lane and ten data lanes. The I^2C module sets parameters for controlling the operation of

the timing generator or a circuit in the driver to a resistor. The timing generator generates a control signal for the drivers and adjusts the data transfer timing.

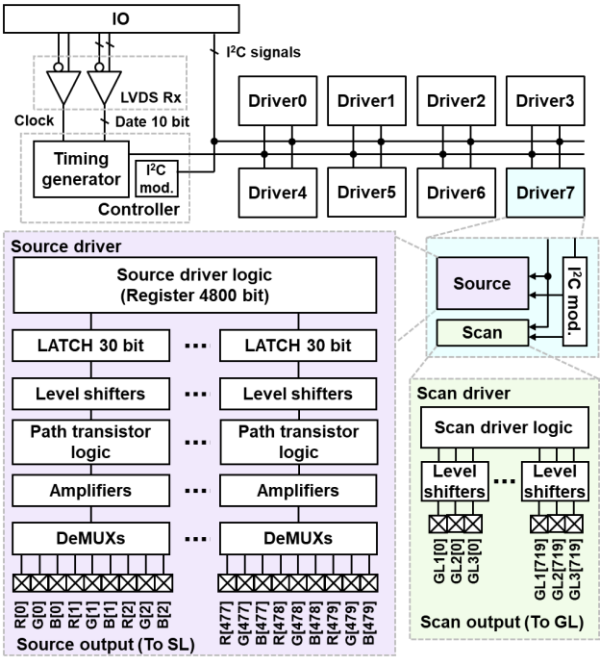

Fig. 6 Block diagram of Si driver block

Figure 6 shows a block diagram of the Si driver block. The driver controls a pixel array with 480 × RGB × 720 pixels. Since the source lines in this prototype display are divided into four, the number of gate lines selected in one frame can be reduced to a quarter in each driver, which means that the horizontal period can be approximately four times as long as that in the structure where the source lines are not divided. Additionally, since all Si drivers are provided under the pixel circuits, the display can be performed at a high frame rate regardless of the size.

4 Pixel

4.1 Pixel Circuit

Figure 7 shows the pixel circuit. All the pixel circuits are formed using OSFETs.

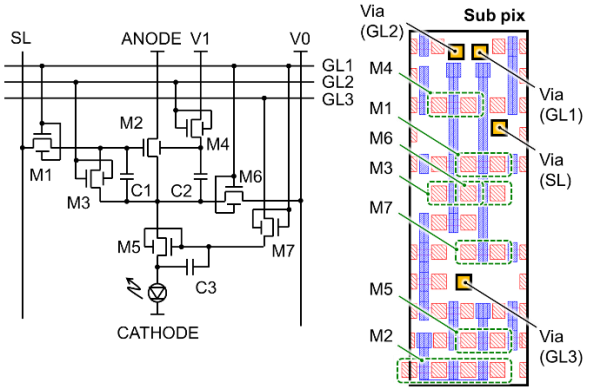

Fig. 7 Pixel circuit diagram and pixel layout

A seven-transistor three-capacitor (7Tr3C) structure is employed where the back gate voltage of the driving transistor (M2) is controlled to perform internal compensation of the threshold voltage, as described in Ref. 14. Since OSFETs have the extremely low off leakage current, the capacitor C2 can store electric charge for compensating the threshold voltage of M2, eliminating the need for compensation in every frame and allowing for low power consumption.

4.2 Pixel Layout

The pixel size is 7.92 μm × 7.92 μm, requiring the FETs to have an ultra-small size and high breakdown voltage in the 7Tr3C pixel circuit of the OLED display. As demonstrated in Fig. 4(B), OSFETs have an ultra-small size and high breakdown voltage. Additionally, the source and scan drivers formed using Si FETs allow data and scanning signals to be supplied from below the pixel region, not from outside the pixel region, so that the degree of freedom of connection is relatively high. Accordingly, the 7Tr3C circuit configuration was obtained, with a definition being as high as 3207 ppi.

5 Results and Discussion

The prototype display has the specifications shown in Table 1.

Table 1 Display Specifications

	Specifications
Screen diagonal	1.5 inches
Resolution	3840 × 2880
Pixel size	7.92 μm × 7.92 μm
Pixel density	3207 ppi
Aperture ratio	62.3%
Coloring method	Side by side
Emission type	Top emission
Source driver	Integrated (bulk Si FET)
Scan driver	Integrated (bulk Si FET)
Structure	OLED/OS/Si (monolithic)

Figure 8 shows an image displayed by the prototype display. The Si driver circuit and the OS pixel circuit were found to operate successfully in the OLED/OS/Si structure, where the OLED devices were formed by photolithographic patterning. Additionally, the luminance was over 5000 cd/m^2.

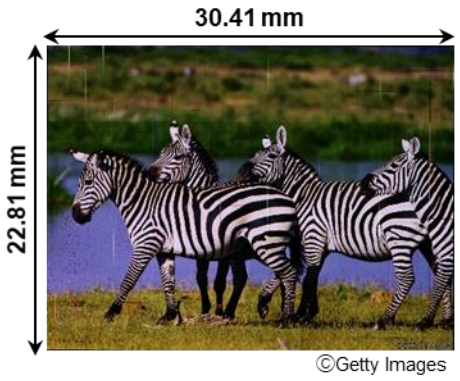

Fig. 8 Picture of the displayed image

The prototype display, in which the 32 drivers can be independently driven, can perform partial rewriting of the screen. In the Si driver circuit, the constant current of the amplifiers of the source driver accounts for a large proportion of the total power consumption. The Si driver has a standby mode for stopping the constant current of the amplifiers to reduce power consumption. Therefore, low power consumption is achieved by combining the standby mode and idling stop driving in each pixel array.

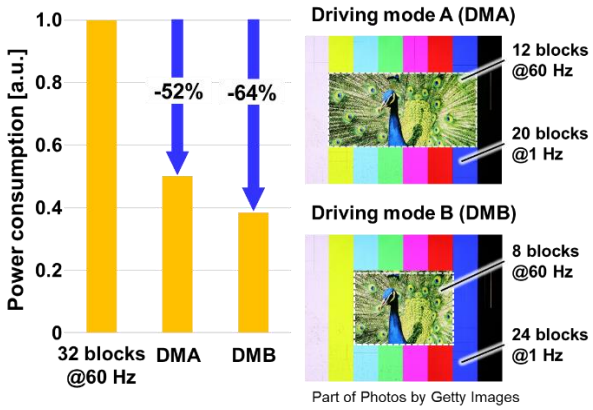

Fig. 9 Power consumption of Si driver circuit

Figure 9 shows the power consumption of the Si driver circuit in the prototype display. The power consumption was measured under the following three conditions: a mode in which a moving image is displayed on the entire screen at 60 Hz (“32 blocks@60 Hz”), a mode in which 12 blocks in the center of the screen are driven at 60 Hz and the other blocks are driven at 1 Hz (DMA), and a mode in which eight blocks in the center of the screen are driven at 60 Hz and the other blocks are driven at 1 Hz (DMB). The power consumption was reduced as more amplifiers were stopped by the standby mode, which revealed that the Si drivers could be driven independently.

6 Conclusion

Using the bulk Si–OS composite LSI technology, we successfully fabricated a prototype OLED display in which miniaturized OSFETs were monolithically stacked over bulk Si FETs. The shot size in the Si process was used to the maximum to achieve a 1.5-inch screen size. Despite a 3840×2880 pixel count and a high definition of 3207 ppi, a high frame rate and low power-consuming operation were possible because divided drivers can be arranged in this display. The OLED devices were formed by side-by-side patterning, allowing the OLED unit to have low power consumption and luminance as high as 5000 cd/m^2.

Therefore, the OLED/OS/Si structure should be an effective technology applicable to XR devices required to have both high definition and large screen size.

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