Ar Plasma Treatment for Highly Stable n^+ region of Self-Aligned Coplanar IGZO TFT

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ABSTRACT

Self-aligned coplanar (SAC) IGZO TFT structure, which has the advantage of a low resistant-capacitance (RC) delay, requires highly conductive n^+ regions which can be realized by plasma treatment. We optimized Ar plasma treatment process conditions to maintain stable n^+ regions and demonstrated SAC IGZO TFT.

1 Introduction

Amorphous IGZO has been a promising material for next-generation displays, such as flexible, transparent, and large-area displays [1, 2]. For high speed and high resolution display, self-aligned coplanar (SAC) IGZO TFT structure is preferred to minimize the parasitic capacitance which is caused by overlap between gate and source/drain (S/D) electrodes [3]. In SAC IGZO TFT structure, a highly conductive n^+ regions can be formed at the S/D regions by selective plasma exposure (Ar, He, and H_2) [4], ion implantation, and diffusion layer (SiO_2 and Si_3N_4) [5, 6]. Among them, plasma treatment is generally used; however, it was reported that the conductivity of the n^+ region was unstable upon air exposure or thermal annealing.

In this paper, we optimized Ar plasma process conditions to maintain the high conductivity of n^+ regions against air exposure and temperature. Besides, the change in electrical properties was negligible even after the plasma enhanced chemical vapor deposition (PECVD) process. Finally, SAC IGZO TFT was demonstrated.

2 Experiment

2.1. Device fabrication

A heavily doped p^{++} silicon with thermally oxidized SiO_2 (200 nm) was used as a substrate. A 40 nm-thick IGZO was deposited by RF sputtering using a ceramic $InGaZnO_4$ target (In:Ga:Zn = 1:1:1 at%) at a RF power of 70 W. The working pressure and Ar/O_2 gas flow rate ratio were 3 mTorr and 30/0 sccm, respectively. The IGZO channel was defined by using standard photolithography processes. Electron-beam evaporated Ti (70 nm) source and drain electrodes (S/D) were defined by lift-off process. To verify the impact of the Ar plasma process, a bottom gated staggered structure was fabricated as a reference device, as shown in Fig. 1(a). Since SAC IGZO TFT usually employs PECVD-SiO_2 as a gate insulator or passivation layer, the electrical properties of IGZO below SiO_2 may change due to high substrate temperature and undesired hydrogen doping during SiO_2 deposition process. Thus, PECVD-SiO_2 (150 nm) was deposited on the reference device to confirm the variations of electrical properties. The substrate temperature was 150 °C, and the gas flow rate ratio of N_2O/SiH_4 was 710/24 sccm. For SAC IGZO TFT fabrication, electron-beam evaporated Ti (40 nm)/Cr (10 nm) was used as a top gate, as shown in Fig. 1 (b). Finally, all devices were thermally annealed in the air at 300 °C. The electrical properties were measured by a semi-conductor parameter analyzer (Keithley 4200-SCS) under ambient conditions.

2.2. Ar plasma process conditions for n^+ region

Ar plasma process was performed on the IGZO surface between S/D using inductively coupled plasma reactive ion etching (ICP-RIE) to increase conductivity as shown in Fig. 1(a). The ICP source power and Ar flow rate were fixed at 2.7 kW and 100 sccm, respectively. The process conditions were optimized by controlling RF power (20, 25, 30 and 50 W) and working pressure (15 and 40 mTorr).

3 Results

Fig. 2 shows the effect of Ar plasma process (15 mTorr, 50 W) on the transfer curve of bottom gated staggered IGZO TFT before and after annealing. The conductivity of IGZO TFT decreased significantly after annealing, so that we speculated that the created n^+ regions were not stable. Given the high etch rate (27 nm/min) at 15 mTorr with 50 W, Ar ion with high energy would penetrate into IGZO bulk and participate in etching IGZO (approximately 10 nm) rather than forming n^+ regions, breaking metal-metal (M-M) bonds at the IGZO surface other than metal-oxygen (M-O) bonds [7].

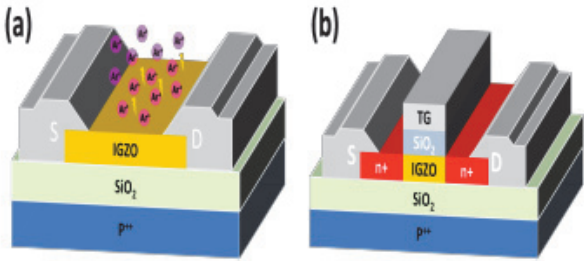

Figure 1. Device configurations for IGZO TFT after Ar plasma process in (a) bottom gated staggered and (b) SAC structure.

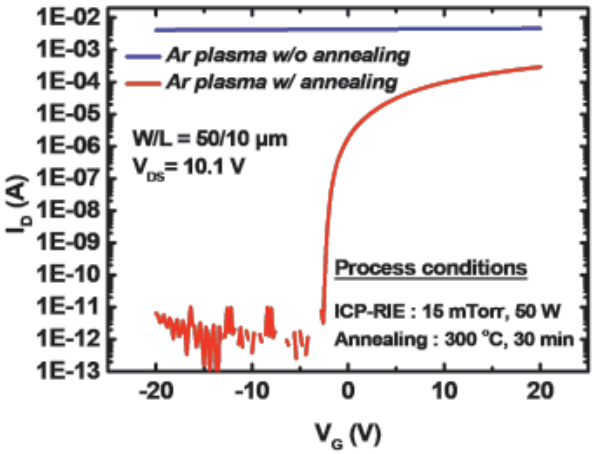

Figure 2. The transfer curves of Ar plasma processed bottom gated staggered IGZO TFT before and after thermal annealing.

Consequently, it is inferred that the n^+ region is easily recovered by annealing when it is formed by breaking M-M bonds at the surface. Therefore, we tried to enhance M-O bond breaking for a stable n^+ regions by reducing Ar ion energy. To verify the conductivity change after annealing according to the Ar ion energy, we increased working pressure affecting the mean free path of Ar ions and decreased RF power to 40 mTorr and 30 W, respectively. At this condition, the etch rate was 8 nm/min, and the conductivity was higher compared to that of IGZO TFT with the initial Ar plasma process (50 W and 15 mTorr), as shown in Fig. 3. To further minimize IGZO etch rate and focus Ar ion energy, especially on the IGZO surface, we decreased the RF power to 25 and 20 W.

However, low RF power may not create sufficient oxygen vacancies of the IGZO surface and thus n+ regions since the Ar ion energy is low. For our samples thevariation of resistivity was small and this indicates that low RF power still forms n^+ regions but with little sacrifice of resistivity. Hereafter, the optimum conditions were defined as

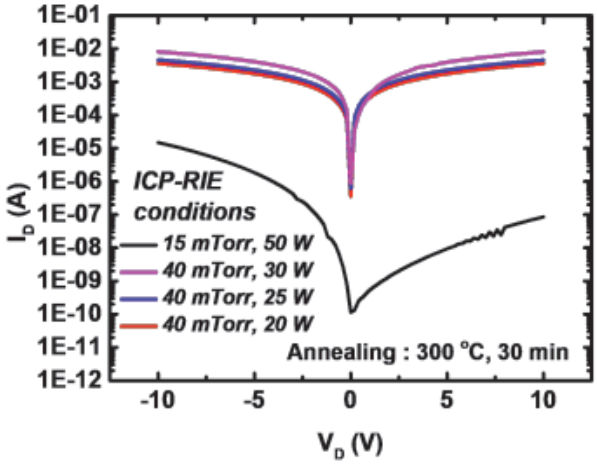

Figure 3. The I-V curves of Ar plasma processed bottom gated staggered IGZO TFT under various conditions.

Table 1. Ar plasma process conditions and resistivity

Working pressure (mTorr)	RF power (W)	Etch rate (nm/min)	Treatment time (s)	Resistivity (Ω*cm)
15	50	27	20	1.35×10^{1}
40	30	8	60	1.8×10^{-2}
	25	5		3.1×10^{-2}
	20	< 0.5		4.05×10^{-2}

working pressure of 40 mTorr and RF power of 20 W to suppress IGZO etching and induce surface treatment.

In general, the electrical properties of IGZO TFT are unstable when the back channel surface is exposed to the air [8]. Therefore, other processes such as treatment or passivation layer were essential to prevent the performance change of IGZO TFT. However, our IGZO TFT after Ar plasma treatment, which was to form stable n^+ regions, showed excellent stability, as shown in Fig. 4. There was no degradation of conductivity even after air exposure to seven days. Note that the current-voltage (I-V) curves were plotted in a linear scale for detailed investigation. Further studies are required to correlate the Ar plasma treatment and electrical stability.

PECVD is a common process to use SiO_2 as a passivation or inter layer dielectric (ILD), but may bring the change in electrical properties of IGZO TFT. Since our intention was to fabricate SAC IGZO TFT, PECVD-SiO_2 was employed as a top gate insulator. Commonly, the characteristics are changed when SiO_2 is deposited on the IGZO channel. This is due to the high process temperature and the effect of hydrogen in the SiH_4

gas of PECVD because this hydrogen, which is known to act as a donor, is more diffused at high process temperature. However, Fig. 5 shows I-V curves in linear scale with negligible change in resistivity even after PECVD process.

As a result, we confirmed that the optimized Ar plasma process conditions formed n+ regions without IGZO etching. Furthermore, the electrical properties of IGZO TFT were maintained stably even after exposure to air, SiO_2 deposition, and thermal annealing.

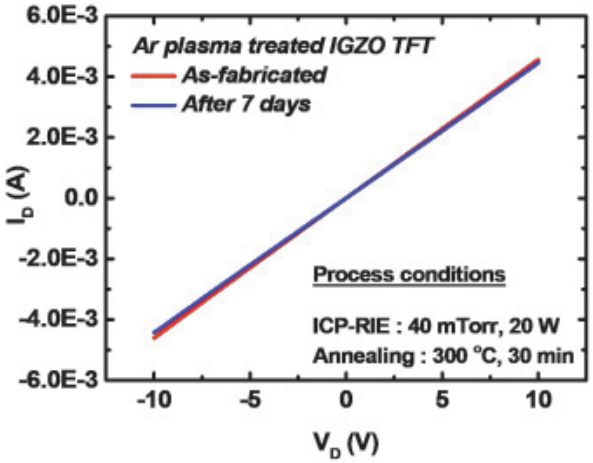

Figure 4. The I-V curves of Ar plasma treated bottom gated staggered IGZO TFT after exposure to air for 7 days.

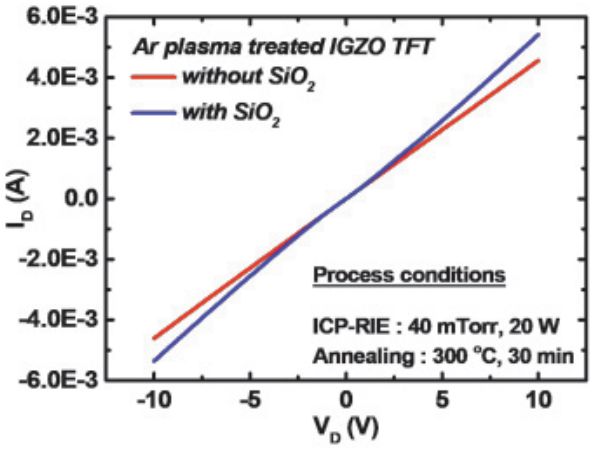

Figure 5. The I-V curves of Ar plasma treated bottom gated staggered IGZO TFT with and without PECVD-SiO_2.

Finally, Ti/Cr top electrode was deposited on top of PECVD-SiO_2 and used as a mask to complete Self Aligned Coplanar IGZO TFT as shown in Fig. 1(b). Fig. 6 shows the transfer curve of SAC IGZO TFT after annealing, suggesting that n^+ regions were successfully formed by Ar plasma treatment.

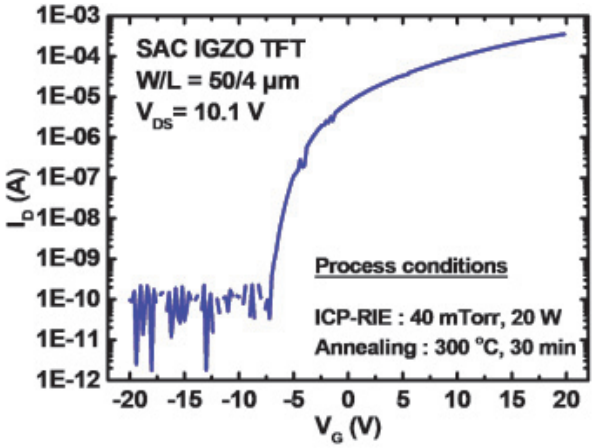

Figure 6. The transfer curve of SAC IGZO TFT.

4 Conclusions

In this study, Ar plasma process conditions were optimized first to induce surface treatment on the IGZO surface rather than ion energy transfer to the bulk. As a result, the high conductivity of IGZO TFT was achieved after annealing. This Ar plasma treatment was also accompanied by the excellent stability against air exposure and PECVD process as well. The electrical characteristic of SAC IGZO TFT, including PECVD and annealing process, reflects the formation of stable n^+ regions.

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