High-reliable Integrated Gate Driver GOA TFT Development under Extremely High Intensity Illumination for Large-Size UHD LCDs Outdoor Display Applications

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Keywords: Amorphous silicon, Gate Insulator, Thin Film Transistor, Black Mura, High Intensity Illumination.

ABSTRACT

We report the unusual black mura reliability behavior in the a-Si TFT when biased under extremely high intensity illumination (> 400000 Cd/cm2). However, the black mura reliability issue is effectively improved by embedding the higher energy band gap (~4.83 eV) design of lower deposited rate N-rich SiNx in the gate insulator. This reliability behavior originated from the injection of electrons in gate electrode, transported and trapped in the electron trap sites of the SiNx/a-Si:H interface. This results can be applicable to the large-sized outdoor displays which are usually exposed to the extremely high intensity illumination.

1 Introduction

TFT-LCD is widely used in display, where gate driver on array (GOA) is the current mainstream with the advantages of low cost and narrow border [1-3]. GOA is based on the control signal provided by the external circuit (CLK, Input and VDD signal). Amorphous silicon (a-Si) TFT technology is suitable for large area applications because of its low cost, low temperature processing and better uniformity. LCDs display using a-Si:H TFT technology as backplane is still the major product in large size display field. However, instability of a-Si is the major factor that hinders stable circuit operation using a-Si TFT. A-Si has meta-stability which is regarded as thermal equilibration process including elements such as band-tail carriers, Hydrogen, weak bonds and dangling bonds, whether it is about defect creation or charge trapping. Degradation of a-Si TFT is inevitable when it is deviated from as deposited equilibrium by the applied bias voltage. Usually bias stressed a-Si TFT shows increase in threshold voltage with time. Circuits using a-Si TFT also show degradation of the circuit characteristics because of the degradation of constituent TFTs.

However, the a-Si:H TFT still have instability problems of threshold voltage shift under current stress operation. After prolonged gate bias stress, the electrical properties are undesirably deviated from the initial values.

The gate bias instability of a-Si:H TFT has been studied for several decades and has generally been explained by two mechanisms: charge trapping within the gate insulator associated with trap sites and defect states created by the breaking of week bonds within a-Si:H. At negative gate bias stress, the threshold voltage commonly shifts toward the negative gate voltage region due to the hole trapping, in which the holes are injected from a-Si:H active layer.

In this study, we report the unusual black mura reliability behavior in the a-Si TFT when biased under extremely high intensity illumination (> 400000 Cd/cm2). However, the black mura reliability issue is effectively improved by embedding the higher energy band gap (~4.83 eV) design of lower deposited rate N-rich SiNx in the gate insulator. This reliability behavior originated from the injection of electrons in gate electrode, transported and trapped in the electron trap sites of the SiNx/a-Si:H interface. This results can be applicable to the large-sized outdoor displays which are usually exposed to the extremely high intensity illumination.

2 Results and Discussion

Fig.1 shows the schematic diagram of proposed GOA driving circuit. This circuit contains some TFTs with small width over channel length (W/L). As channel length (L) has little impact on device stability, W/L can amplify with same ratio to improve the process uniformity. Duty ratio of GOA clock signal (CLK) could be modified to improve the TFT stability after long time operation and guarantee our GOA circuit performance. In the GOA driver circuit, TFT plays important role. TFT performance may change due to fluctuations in the production process should also be reflected in the simulation.

On the basis of this study, we analyzed the underlying mechanism of this TFT reliability issue, showing that the electrons from contact gate metal played a key role in supplying electrons into the gate insulators, which are trapped at the interface between gate insulator and a-Si:H active layer. This is more obvious TFT reliability issue in a low work function gate metal structure of Al (4.0−4.3 eV), compared to the high work function of Cu (4.5−5.2 eV) as shown in Fig.2.

Fig. 3 shows the schematic energy band diagrams under negative gate bias stress with high intensity illumination in a-Si:H TFT of (a) a normal gate insulator (GI SiNx) scheme, and (b) a low deposited rate N-rich GI SiNx layer inserted in the gate insulator.

We consider that the unusual black mura reliability behavior could be strongly related to the injection of electrons from gate metals under high intensity illumination bias stress. However, in the lower deposited rate N-rich SiNx layer inserted TFT within the gate

insulator layer, the transport of electrons from gate electrode to trap sites is blocked by the higher potential energy barrier.

In Fig.4, we show that (a) The absorption spectrum in a-Si:H TFT of a high deposited rate GI SiNx (GH) layer, and (b) its energy band-gap (Eg) calculated by the absorption spectrum results. (c) Energy band-gap structure measured/calculated by absorption spectrum of GI layer.

In Fig. 5, we show that (a) Schematic diagram of the high intensity illumination reliability test. (b) 500hr high intensity illumination RA result of TFT-LCDs display with a-Si:H TFT based on (b) high deposited rate gate insulator (with Black Mura) and (c) embedding the N-rich lower deposited rate gate insulator (without Black Mura).

In Fig.6, we show that (a) Schematic a-Si:H TFT structure used in this study, (b) the related table for bond strengths and of Si-H, N-H, Si-Si, and Si-N, (c) the related table for chemical bonding contents of Si-H and N-H,(d) Schematic TFT structure of the a-Si:H/GI, (e) the Von margin results with different high deposited rated GI (GH) thickness.

3 Conclusions

We report the unusual black mura reliability behavior in the a-Si TFT when biased under extremely high intensity illumination (> 400000 Cd/cm2). However, the black mura reliability issue is effectively improved by embedding the higher energy band gap (~4.83 eV) design of lower deposited rate N-rich SiNx in the gate insulator. This reliability behavior originated from the injection of electrons in gate electrode, transported and trapped in the electron trap sites of the SiNx/a-Si:H interface. This results can be applicable to the large-sized outdoor displays which are usually exposed to the extremely high intensity illumination.

4 Acknowledgements

This work was supported by HKC optoelectronics.

References

[1] H.N. Cho, Y.H Jang, S.Y. Yoon, B. Kim, M.D Chun, S.C. Choi, K.S. Park, T. Moon, H. Y. Kim, C.I. Ryoo, N.W. Cho, S.H. Jo, C.-D. Kim, and I.-J. Chung “a-Si TFT Gate Driver Circuit Having Dual Pull-down Structure with Shared Node Controller”, IDW Digest, pp.285-288, 2006.

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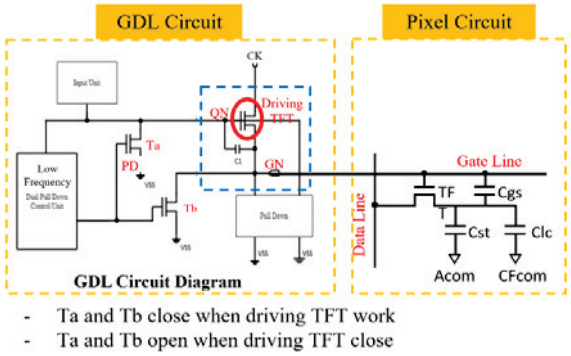


Fig. 1 Schematic diagram of proposed GOA driving circuit.

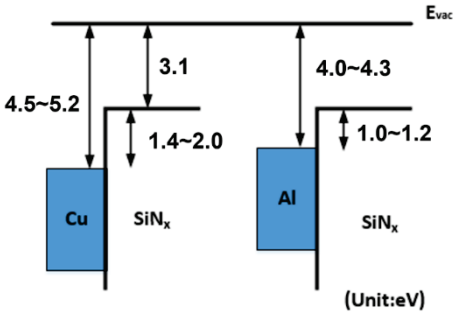


Fig. 2 Schematic energy band diagrams of Cu and Al gate metal/GI SiNx gate insulator structure.

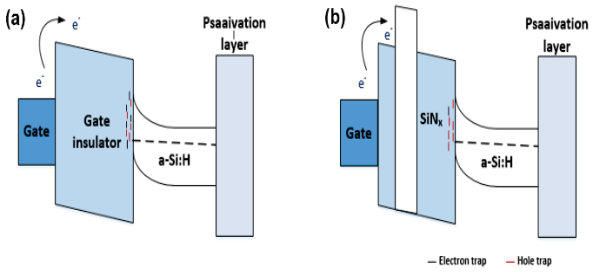
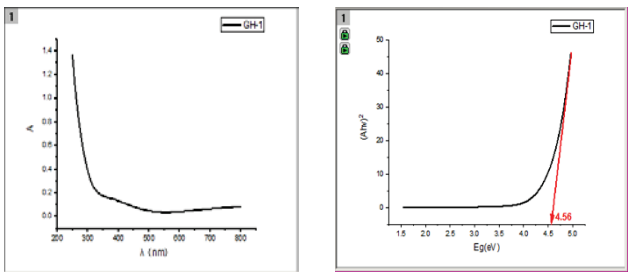
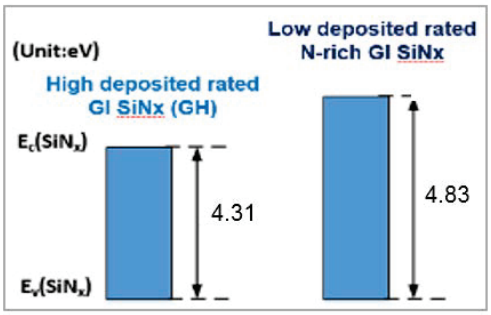


Fig. 3 Schematic energy band diagrams under negative gate bias stress with high intensity illumination in a-Si:H TFT of (a) a normal gate insulator (GI SiNx) scheme, and (b) a low deposited rate N-rich GI SiNx layer inserted in the gate insulator.

(a) (b)



(c)



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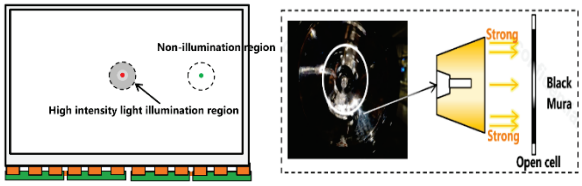
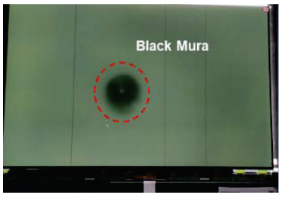
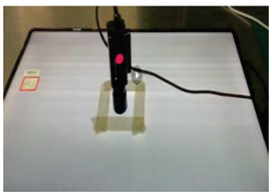
(a)



(b)



(c)



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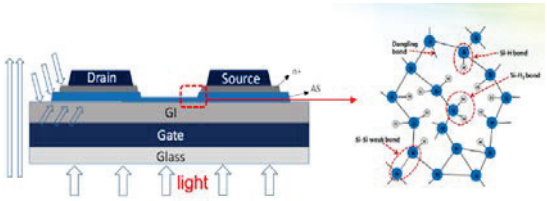
(a)



(b)

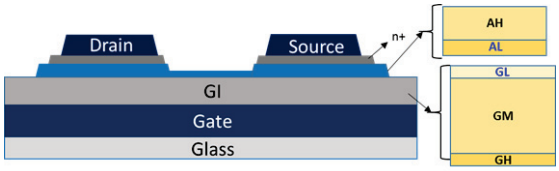
Table I. Bond strengths of Si–H, N–H, Si–Si, and Si–N.

Bonding	Bond strength (kcal/mole)
Si–H	71.34
N–H	75
Si–Si	78.1
Si–N	105

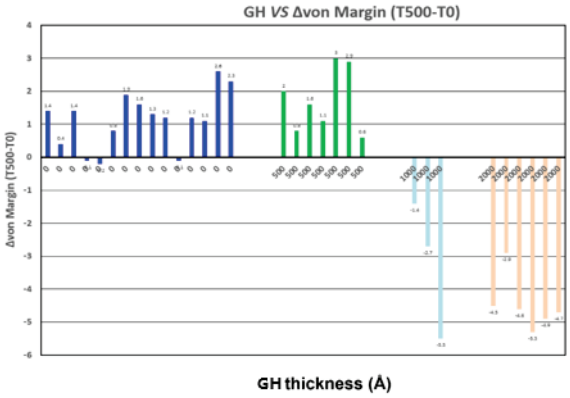
(c)

	R.I.	Dep. Rate	Stress	N-H(%)	Si-H(%)
		Å/min (Ratio)	E9 dyne/cm^2	%	%
GH	1.92	1	3.8	~18%	~18%
GM	1.88	0.75	-0.4	~18%	~9%
GL	1.87	0.5	-2.8	~30%	~2%

(d)



(e)



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