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Thermally Stable Ternary Amorphous Oxide Semiconductors for HfO_2-based Ferroelectric Field-Effect Transistor Memories

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ABSTRACT

We have proposed ternary AOS in views of compatibility with ALD process and thermal stabilities for HfO_2-based ferroelectric memories. Our AOS-FET achieved mobility over 20 cm^2/Vs under maximum annealing temperature of 600°C. This paper discusses FET performance with AOS deposited by sputtering or ALD, and potential for ferroelectric device applications.

1 Introduction

Ferroelectric field-effect transistors (FeFETs) with HfO_2-based material [1] have been attracting researchers' attention as a candidate for high-density non-volatile memories; for example, scalability of device structure, CMOS process compatibility, low-power consumption, and high-speed operation. Recently, a three dimensional (3D) vertical-FeFET inspired by the 3D-NAND flash memories has been proposed [2]. Polycrystalline silicon (poly-Si) is commonly used as a channel material in 3D-NAND memories; however, there are serious problems with degradation in device performance due to an interfacial layer between the channel and ferroelectric gate insulator in the case of HfO_2-based FeFETs. In addition, further stacking of memory cells is limited by small read-current due to low-mobility of the thin poly-Si channel. To solve these issues, oxide semiconductors have been proposed as a new channel material for HfO_2-based FeFETs [3, 4, 5, 6]. Amorphous oxide semiconductors (AOSs) can potentially realize an interfacial layer free structure, scalability of channel thickness, and further low-power consumption, which will maximize the performance of HfO_2-based FeFETs [3].

Recently, we have reported a vertical-FeFET using polycrystalline In_2O_3 channel derived by atomic layer deposition (ALD) [4]. However, the In_2O_3-based polycrystalline channels have problems in grain boundary-induced poor uniformity in short-channel device and controllability of threshold voltage (V_{th}) against process temperature and atmosphere. In the FeFET fabrication, crystallization temperatures of ferroelectric HfO_2-based material are much higher than conventional process temperature of AOS thin-film transistor (below 400℃). Annealing temperatures above 500℃ is required to induce sufficient ferroelectricity. Thus, we consider stabilities of amorphous phase with device performance after high-temperature process as essential properties of AOS material for FeFET. In addition, these thermal stabilities of AOS are practical for flexibility of device design and extending the process window of FeFET integration. In the case of conventional In-Ga-Zn-O (IGZO) composition [7], high-temperature annealing induces the degradation in electron mobility [8]. The IGZO have a specific crystalline phase such as $InGaZnO_4$ which results in a lowering of crystallization temperature. Therefore, an optimum material must be designed in views of the compatibility with the process of ferroelectric HfO_2 (Fe-HfO_2) and thermal stabilities of electrical property to apply AOS in FeFET as a channel material.

To apply AOSs to vertical-FeFET, the deposition method must be changed from the conventional sputtering to the ALD method. When we deposit complex oxides such as quaternary AOS system such as IGZO by ALD, three kinds of precursors are required, and the super-cycle method is used to stack each oxide layer [9]. Thus, there are some problems about complicated ALD process and poor controllability of composition ratio in the case of having many metal-cations in the AOS system. Unlike conventional sputtering methods, simpler material systems such as ternary system are preferred than quaternary AOS in ALD process.

Based on these backgrounds, we propose ternary AOS toward HfO_2-based vertical-FeFET, as shown in Fig. 1. In this study, we designed In_2O_3-based ternary AOS system composed by two types of metal-oxides. This paper discusses the thermal stabilities of designed AOS and its FET performance, demonstration of ferroelectric devices, and the basic FET characteristics with ALD-derived channel.

2 Experiment

2.1 Fabrication process of FET using AOS channels

To fabricate the FETs, 10-nm-thick AOS channels were deposited on 85-nm-thick SiO_2/n^+-Si substrate by RF magnetron sputtering or plasma enhanced ALD (PEALD). The oxide channels were patterned by photolithography and wet-etching or lift-off process. To

investigate stabilities against high-temperature process, AOSs were annealed at 300 to 700°C in air atmosphere for 60min. A rapid thermal annealing (RTA) at 500°C for 15 sec in N_2 was performed on some samples. The Pt/Mo stacked thin films as source/drain (*S*/*D*) electrodes were deposited by RF magnetron sputtering and patterned using photolithography with lift-off process. As the passivation layer, AlO_x was deposited by RF magnetron sputtering. After all these processes, the FETs were annealed at 350°C in N_2 atmosphere. The device structure is provided in Fig. 2 (a).

2.2 Fabrication process of planar-type FeFETs and ferroelectric capacitors

The 15-nm-thick Zr-dpoed HfO_2 (HZO, 1:1 at.%) thin films were deposition by ALD on TiN/n^+-Si substate. The 10-nm-thick AOS channel was deposited on HZO/TiN/Si structure. The AOS were patterned by photolithography and wet-etching. A 20-nm-thick AlO_x buffer-layer under *S*/*D* pad was deposited by RF magnetron sputtering and patterned by lift-off process to suppress gate leakage current. RTA at 500°C for 10 sec in N_2 was performed to crystalized HZO thin films. The Pt/Mo stacked thin films as *S*/*D* electrodes were deposited by RF magnetron sputtering and patterned using photolithography with lift-off process. As the passivation layer, AlO_x was deposited by RF magnetron sputtering. After all these processes, the samples were annealed at 350°C in N_2 atmosphere. Through these processes, FeFET and metal-ferroelectric-semiconductor (MFS) capacitors with AOS/HZO/TiN structure were fabricated at the same time.

3 Results and Discussion

3.1 FET performance of thermally stable AOS

In this work, In-Al-O (IAO), In-Zn-O (IZO), and In-Ga-O (IGO) systems were considered as candidate ternary AOS channel material for FeFET and ALD deposition. Conventional sputtering method was used for AOS deposition before ALD application to investigate its basic physical properties with the effects of dopant elements into In_2O_3. We consider that Al_2O_3, ZnO, and Ga_2O_3 can be deposited by ALD method using general precursors such as trimethylaluminium, diethylzinc, and trimethylgallium, respectively. At first, we investigated the effect of RTA in N_2 on AOS, because it corresponds to typical crystallization process of Fe-HfO_2. Figure 2 (b) shows transfer characteristic of FET with 10-nm-thick IAO, IZO, and IGO under RTA process. Note that the carrier concentration before annealing process is low. The IAO-FET was poor as a channel material due to its small on-current and high-subthreshold swing (*SS*). We consider that high Al_2O_3-doping to In_2O_3 is effective to suppress the crystallization and generation of excess free electrons; however, there is a trade-off relationship between the doping amount of Al_2O_3 and FET performance. In case of IZO, high-mobility over 40 cm^2/Vs and switching behavior were confirmed; however, V_{th} showed a lower value. In contrast to IZO and IAO, IGO-FET showed good electrical characteristics such as V_{th} near 0 V, field effect mobility (μ_{FE}) of 22 cm^2/Vs and *SS* of 97mV/decade. Compared with IZO and IGO, the oxygen bond dissociation energy of Ga-O is higher than Zn-O, suggesting that IZO easily increase carrier concentration due to formation of oxygen vacancies. The high-mobility AOS tend to have lower activation energies than low-mobility AOS [10]. In addition, carrier concentration of high-mobility AOS such as IZO is sensitive to change in doping concentration (hydrogen impurities and oxygen vacancies). Thus, the IGO system is preferable for the Fe-HfO_2 process where high-temperature annealing is performed in N_2 atmosphere. From these results, we demonstrated that Ga_2O_3 doping into In_2O_3 can suppress excessive oxygen vacancy due to the RTA process and contribute to achieve stable FET operation.

Based on the results of Fig. 2 (b), we focused on the IGO system and evaluated the thermal stability of the amorphous phase. Fig. 3 shows XRD patterns of as-deposited and annealed (a) In_2O_3 and (b)IGO thin films. Diffraction peaks from the bixbyite structure were observed from In_2O_3 with and without annealing. In contrast, the IGO annealed below 600°C were characterized as having remained in the amorphous phase because only the halo peak was observed. This result suggests that the Ga_2O_3 doping can suppress the crystallization of In_2O_3 phase and maintain the amorphous phase below 600°C.

Next, we evaluated the annealing temperature dependency on FET characteristics. Fig. 4 (a) shows transfer characteristic of FET with IGO channel annealed at 300 to 700°C. The IGO-FET with all annealing temperature showed switching behavior and stable V_{th} close to 0 V. Furthermore, we confirmed that the μ_{FE} over 20 cm^2/Vs and the *SS* below 80 mV/decade were maintained up to 600ºC. In contrast, degradation in μ_{FE} and *SS* were observed in IGO annealed at 700°C. We consider that this is due to grain boundary scattering caused by crystallization of the IGO channel. Based on these results, we successfully designed a ternary AOS that combines thermal stabilities up to 600°C of amorphous phase and FET performance. This temperature range has good compatibility with the fabrication temperature of ferroelectric HZO [11].

Furthermore, we tried to deposit IGO channel by ALD. To obtain optimal chemical composition ratio of IGO by ALD, the cycle ratio between InO_x and GaO_x layers were controlled. Fig. 4 (b) shows transfer characteristic of FET with sputter and ALD-deposited IGO channels. The channel film thickness and annealing temperature are 10 nm and 500°C, respectively. The FETs with ALD-IGO channel showed almost the same transfer characteristics as sputter-IGO. In addition, we confirmed

that composition ratio of ALD-IGO is almost the same as sputter-IGO, and its amorphous phase is remained after annealing process. This result suggests that the IGO system has compatibility for ALD process.

3.2 Amorphous IGO application to HfO_2-based ferroelectric devices

The MFS capacitor and FeFET were designed to confirm the compatibility of our IGO channel with the Fe-HfO_2 process, as shown in Fig. 5 (a) and (b), respectively. During the fabrication of these devices, RTA at 500°C in N_2 was performed on HZO thin films with IGO capping. This is because the ferroelectric orthorhombic phase of HZO is efficiently induced when the AOS such as IGZO is used as the capping material [3]. Note that IGO channel maintained amorphous phase under this RTA process. Fig. 5 (c) shows polarization (*P*) - voltage (*V*) and current density (*J*) - *V* characteristics of fabricated MFS capacitor. A counterclockwise *P*-*V* loop and switching current in *J*-*V* curve from polarization switching were observed from the MFS capacitor with IGO and HZO. These results ensure that MFS capacitor exhibits clear ferroelectricity with a remanent polarization value of about +9 μC/cm^2 and -7 μC/cm^2. Fig. 5 (d) shows capacitance (*C*) -*V* characteristic of fabricated MFS capacitor. The *C*-*V* characteristic showed difference in capacitance values between negative and positive voltage region attributed to depletion and accumulation of IGO semiconductor. In addition, a counterclockwise hysteresis with two capacitance peaks at negative and positive voltage region from polarization switching were also observed. We consider that the low-voltage operation of FeFET is expected from a coercive voltage (V_c) of IGO/HZO/TiN gate stack is below 3 V. The *P*-*V* and *C*-*V* characteristics are typical property of MFS capacitor induced by ferroelectricity excluding the effect of leakage current [2, 3, 6].

Finally, the hysteresis measurement of FeFET with IGO channel and HZO gate insulator was performed, as shown in Fig. 5 (e). The FeFET showed counterclockwise hysteresis behavior in the transfer characteristics. The ΔV_{th} between forward and reverse sweep was 0.49 V. The current peaks around V_c were observed in gate currents in negative and positive gate-voltage region, which correspond to the polarization switching under gate to source electrode and channel region, respectively. Note that this hysteresis behavior in Fig. 5 (e) is a short-term characteristic because erase operation is not expected in n-channel oxide semiconductors with a long channel length (micro-order) [3]. This problem in erase operation can be solved by employing a short channel length such as 50 nm [4]. We consider that the insensitivity of our IGO against high-temperature process and RTA can be expected to suppress channel shortening [12] in vertical FeFET. These results demonstrate that IGO has compatibility with HfO_2-based memory devices.

4 Conclusions

Ternary AOS material has been designed in views of thermal stability against high-temperature annealing and compatibility with ALD process toward 3D vertical-FeFET applications. The use of the IGO system ensures thermal stabilities of excellent FET performance with amorphous phase up to 600°C, which is sufficient as the crystallization temperature of Fe-HfO_2. We also demonstrated ALD deposition of IGO and FET operation using it as a channel. In addition, clear ferroelectricity was obtained from MFS capacitors and FeFETs using IGO channels and HZO. We believe that IGO is a promising candidate channel material for HfO_2-based vertical-FeFETs and 3D-integrated device application.

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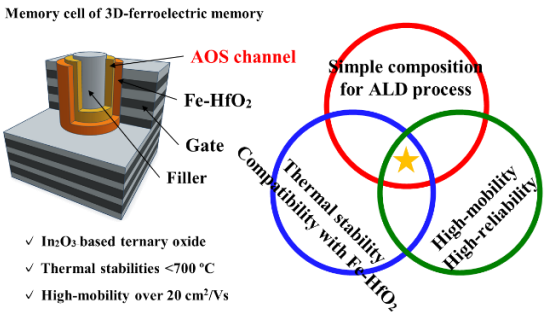

Fig. 1 Material design of ALD compatible and thermally stable AOS toward HfO_2-based vertical-FeFET.

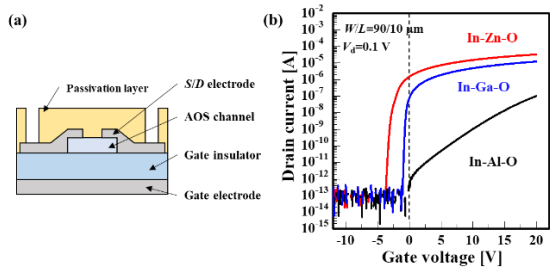

Fig. 2 (a) Illustration of device structure of the FETs using AOS channel. (b) Transfer characteristics of amorphous IAO, IGO, and IZO-FETs with RTA.

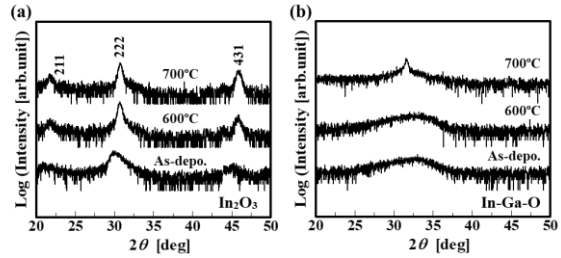

Fig. 3 XRD patterns of 50-nm-thick (a) In_2O_3 and (b) IGO thin films with various annealing temperature.

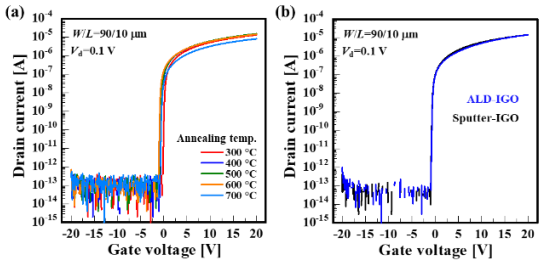

Fig. 4 (a) Transfer characteristics of IGO-FETs with various annealing temperatures. (b) Transfer characteristics of IGO-FETs with ALD (bule line) and sputter (black line) -derived channels.

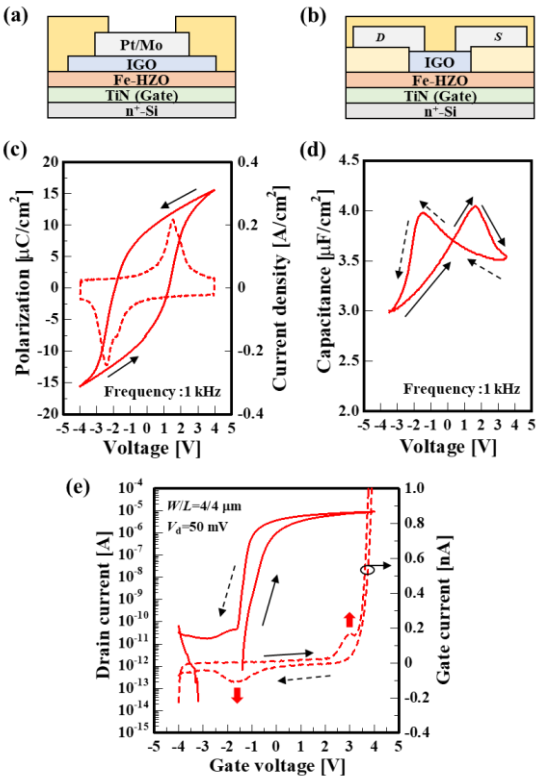

Fig. 5 Device structures of (a) MFS capacitor and (b) planar-type FeFET with IGO channel and HZO. The (c) *P-V* with *J-V* and (d) *C-V* characteristics of MFS capacitor. (e) Hysteresis behavior in transfer characteristics of FeFET using IGO channel and HZO with gate leakage currents.