A New Integrated Scan/Emission Driver with Adjustable Emission Pulse Width using 3-phase Clock Signals

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ABSTRACT

We propose a new integrated scan/emission driver circuit using 3-phase clock signals. The scan/emission part shares the clock lines, and no additional dummy stage is needed. The scan output is pulled up by both pull-down and -up TFTs to reduce the rising time and the size of the pull-up TFT. In addition, the emission output pulse width can be adjusted in 1 frame time. Therefore, the proposed circuit is applicable to reduce power consumption and improve image quality for high-resolution AMOLED displays. The simulation results verified the stable operation during the 1 frame time.

1 Introduction

Low-temperature polycrystalline silicon (LTPS) thin-film transistors (TFTs) can make smaller size layout spaces because of their higher mobility. Therefore, the LTPS backplane is regarded as one of the best options in active-matrix organic light-emitting diode (AMOLED) displays with high resolution and high frame rates. However, there are some issues with LTPS TFT with luminance nonuniformity due to non-uniform electrical characteristics of threshold voltage (V_{TH}) and mobility variation. The luminance nonuniformity caused by nonuniform electrical characteristics of TFT needs to be compensated [1]. The emission signal is required to turn OLED off during the compensation period [2]. The progressive emission method has a long 1H time and lowers dynamic power consumption compared to the simultaneous emission method [3]. It is preferred for high-resolution and high frame rate displays. The emission driver circuit is required for applying the progressive emission method.

The scan driver and the emission driver, called gate-driver-on-array (GOA), are normally located on both sides of the panel. The space occupied by GOA circuits is one of the factors to affect bezel size. In addition, the resistive-capacitive (RC) load of the gate line becomes larger with the increased pixel density. In order to implement a high-resolution display, a small-sized GOA circuit is required to reduce the area without degrading the driving capability.

Adjusting the emission time can improve the grayscale capability at a low luminance level [4]. In addition, it can reduce the power consumption which is the same effect as active-matrix liquid crystal displays (AMLCDs) dimming technology [5], and prevents image distortion of the display screen [6]. Therefore, it is adaptable to reduce power consumption and improve image quality for AMOLED displays.

We propose a new integrated scan/emission driver circuit using 3-phase clock signals. The size of pull-up TFT is reduced because the scan signal is pulled up by both pull-down and -up TFT, using 3-phase clock signals. In addition, the emission output pulse width can be adjusted in 1 frame time. The proposed circuit is applicable to reduce power consumption and improve image quality for high-resolution AMOLED displays.

2 Integrated scan/emission driver circuit

Fig. 1 shows the circuit structure of the proposed integrated scan/emission driver. The proposed circuit is composed of 18 TFTs, 4 capacitors, 3 clock signals (CLK1~3), and power lines (VGH and VGL) as shown in Fig 1 (a) SCAN[n] is generated using 5T2C (T1, T3, T5, T6, T7, C1, and C2), CR[n] is generated additional 4T1C (T2, T4, T8, T9, and C3) and others (T10~18 and C4) for EM[n]. The SCAN[n] signal pulls down the EM [n] and the CR[n] signal acts as a trigger to pull up the EM[n]. All CLKs and output signals (CR[n], EM[n], and SCAN[n]) are operated within a swing range from -5 V to +15 V. The proposed integrated scan/emission driver has total 6 operational periods, with pre-charging, bootstrapping and reset period repeated twice. The proposed circuit requires two start input signals (VST1 and VST2) with different timings as shown in Fig. 1 (b). The advantage of using two start signals is that additional dummy stages are not required as shown in Fig. 1 (c).

2.1 Operation process

A. Pre-charging period (SCAN[n])

SCAN[n-1] and CLK1 become VGL to turn T2 on. SQ node voltage is pre-charged to low voltage. SQB node voltage is charged to VGH through T4. Because CLK2 is still VGH, SCAN[n] is maintain high voltage.

B. Bootstrapping period (SCAN[n])

CLK1 becomes VGH to turn T2 off, SQ node is a floating state in this period. Therefore, the SQ node is bootstrapping using C3, as CLK2 becomes VGL. SQB node voltage is held VGH by C1. The SCAN[n] is pulled down by T9. SCAN[n] goes into the input of the EM[n]

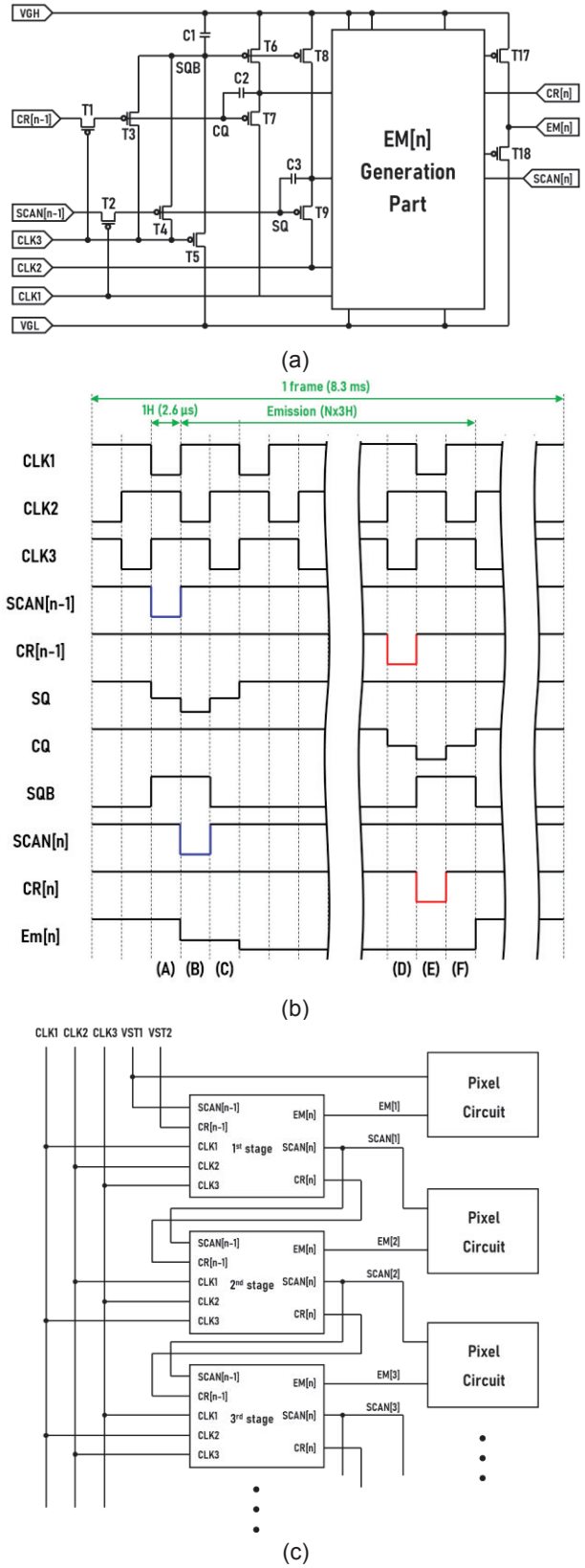


Fig. 1 Proposed integrated scan/emission driver : (a) circuit schematic, (b) timing diagram, and (c) block diagram.

generation part and EM[n] is pulled down by T18.

C. Reset (SCAN[n])

CLK3 becomes VGL to turn T5 on, and the SQB node voltage is discharged to low voltage. CLK2 becomes VGH and SQ node voltage is increased by C3, however, it is low enough to turn on T9 because the SQ node is bootstrapped down before. Therefore, both T8 and T9 pull up SCAN[n]. After this period, T9 is turned off because VGH goes into the SQ node through T2 whenever CLK1 becomes VGL.

D. Pre-charging (CR[n])

CR[n-1] and CLK3 become VGL to turn T1 on and CQ node voltage is discharged to low voltage. CQ node voltage turns T3 on, so SQB node voltage is charged to VGH. Because CLK1 is still VGH, CR[n] is maintain high voltage.

E. Bootstrapping period (CR[n])

CLK3 becomes VGH to turn T1 off, so the CQ node is a floating state. Therefore, the CQ node is bootstrapping using C2, as CLK1 becomes VGL. SQB node voltage is held VGH by C1. As a result, CR[n] is pulled down by T7. CR[n] and C[R] acts as a trigger to pull up the EM[n].

F. Reset (CR[n])

CLK1 becomes VGH and CQ node voltage is increased by C2, however, it is low enough to turn on T7 because the SQ node is bootstrapped down before. Therefore, T7 pulls up C[n] to VGH. After this reset period, T7 is turned off because VGH goes into the CQ node through T1 whenever CLK3 becomes VGL. To keep SCAN[n] and CR[n] at VGH, the SQB node is pulled down by CLK3 at 30% duty of the clock signal using T5. And EM[n] is pulled up when CLK3 goes VGL. In addition, EM[n] pulse width can be adjusted by 3N x 1H time increments.

2.2 Simulation Condition

We simulated the proposed integrated scan/emission driver circuit using the Smartspice circuit simulator with RPI (level = 36) model. The frame frequency was 120Hz, and the 1H time was 1.9 µs based on the QHD (1440 (horizontal) × RGB × 3200 (vertical)) resolution. All TFTs have the same channel length of 3 µm and various channel widths, considering a stable operation. The channel width of pull-down TFT (T9 and T18) was designed to 40 µm to discharge the SCAN[n] and EM[n] gate lines, respectively. Although T6 is used as both pull-down and -up TFT, since there is no gate line load on CR[n], the channel width of T6 can be designed to 10 µm. All capacitors in the proposed circuit were set 0.1 pF. Only 1 pull-up TFT (T17) width size was designed to 20 µm to charge the EM[n] gate line load. The width of T8

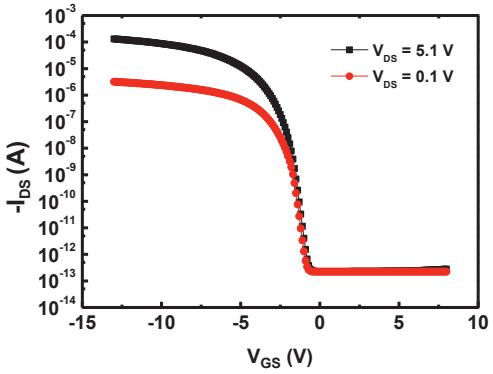


Fig. 2 I-V transfer characteristics of a LTPS TFT.

was set to 4 μm as same as the other switching TFTs because SCAN[n] is pulled up by both T8 and T9. Consequently, T9, T17, and T18 width size is a dominant effect on the proposed circuit driving capability. A worst-case clock load line condition (RC = 54 ns) was applied to verify the final stage of the proposed circuit structure using the distributed RC model [7]. Fig. 2 shows the I-V transfer curves of the LTPS TFT used in the proposed scan driver circuit. The simulated electrical characteristics of the LTPS TFT exhibited a V_{TH} of −2.56 V, a field-effect mobility of 105 $cm^2/V{\cdot}s$, and a subthreshold slope of 0.23 V/decade.

3 Results and Discussion

Fig. 3 shows that the proposed circuit can drive the stable output voltage of SCAN[n] with V_{TH} variation of -1.56 V to -5.56 V. The maximum rising and falling times of SCAN[n] were 400.6 ns and 685.1 ns, respectively. The rising time increase (41.7 %) is less than the falling time increase (84.6 %). The EM[n] was simulated at 20 %, 40 % 60 %, 80% of 1 frame time, as shown in Fig. 4 (a). Fig. 4 (b) exhibits the multistage operation of the proposed circuit. The ripple voltages for the EM[n] and SCAN[n] nodes of the last 5 stages were not generated. Therefore, the stable voltage was supplied to the switch TFT of the pixel circuit without multi-output and voltage degradation. Simulation results prove that adjustable emission signal and stable scan signal can be generated from the proposed circuit structure.

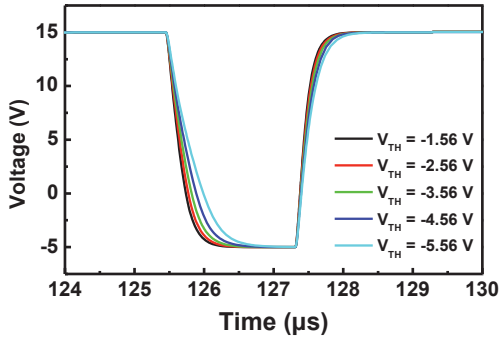
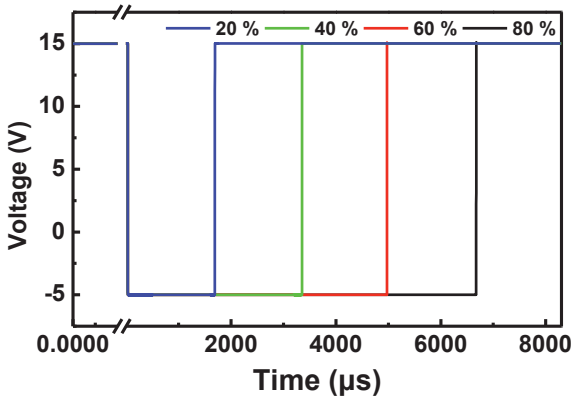
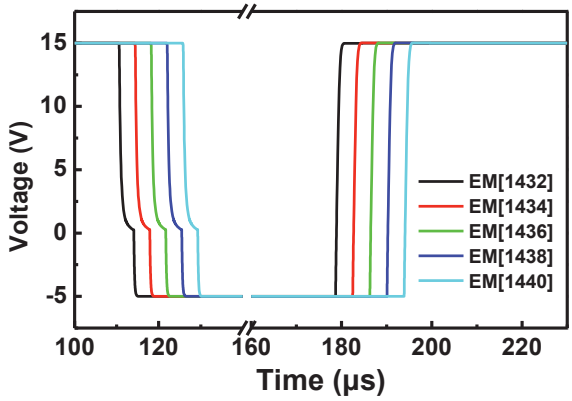
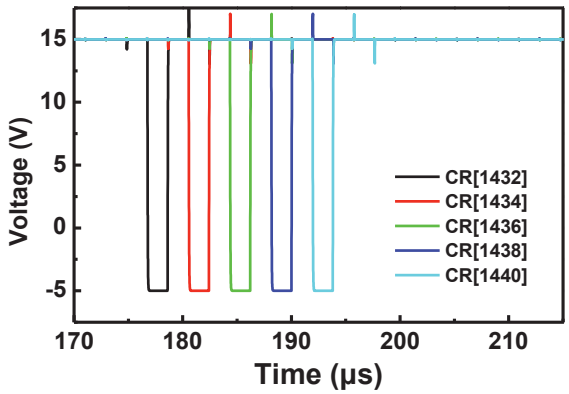


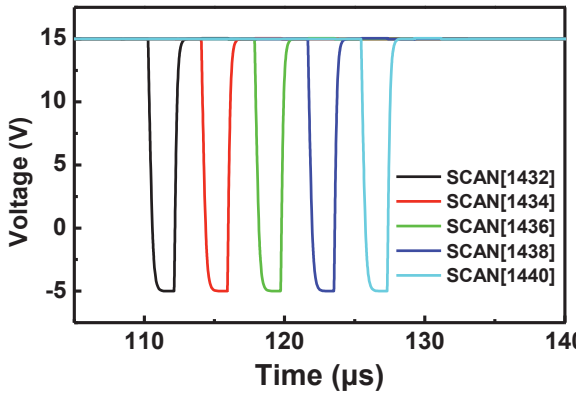
Fig. 3 Simulation voltage waveforms of SCAN[n] as V_{TH} varies from -1.56 V to -5.56 V.



(a)







(b)

Fig. 4 Simulation voltage waveforms : (a) EM[n] adjusted in 1 frame time, (b) EM[n], CR[n] and SCAN[n] in a multistage structure.

4 Conclusion

In this paper, we proposed a new integrated scan/emission driver circuit using 3-phase clock signals. The simulation results for the proposed circuit verified output signals are stably pulled down to -5 V (VGL) and pulled up to 15 V (VGH) during the operation process. The rising time increase was confirmed by half compared to the falling time increase with V_{TH} variation of -1.56 to -5.56 V because SCAN[n] is pulled up by both pull-down and -up TFTs. Therefore, the proposed circuit can drive stable scan output signals and reduce the size of the pull-up TFT of SCAN[n]. It can be applied to realize narrow bezel displays by means of the scan/emission part sharing the clock lines and no additional dummy stage. In addition, the emission output pulse width can be adjusted by 3N x 1H time increments in 1 frame time. Consequently, the proposed circuit is applicable to reduce power consumption and improve image quality for AMOLED displays.

References

[1] J. Oh, J.-H. Kim, J. Lee, E. K. Jung, D. Oh, J. Min, H. Im, and Y.-S. Kim, “Pixel circuit with P-type low-temperature polycrystalline silicon thin-film transistor for micro light-emitting diode displays using pulse width modulation,” *IEEE Electron Device Lett.*, vol. 42, no. 10, pp. 1496–1499 (2021).

[2] A. Nathan, G. R. Chaji, and S. J. Ashtiani, “Driving Schemes for a-Si and LTPS AMOLED Displays,” J. Disp. Technol., vol. 1, no. 2, pp. 267–277 (2005).

[3] N. H. Keum, K. Oh, S. K. Hong, and O. K. Kwon, “A Pixel Structure Using Block Emission Driving Method for High Image Quality in Active Matrix Organic Light-Emitting Diode Displays,” J. Disp. Technol., vol. 12, no. 11, pp. 1250–1256, 2016, doi: 10.1109/JDT.2016.2594835.

[4] T. Shiga and S. Mikoshiba, “49.2: Reduction of LCTV Backlight Power and Enhancement of Gray Scale Capability by Using an Adaptive Dimming Technique,” SID Symp. Dig. Tech. Pap., vol. 34, no. 1, p. 1364 (2003).

[5] C. C. Lai and C. T. Tsai, “Backlight power reduction and image contrast enhancement using adaptive dimming for global backlight applications,” IEEE Trans. Consum. Electron., vol. 54, no. 2, pp. 669–674 (2008).

[6] D.-W. Kim, W. J. Choe, K.-S. Shin, B.-H. Kim, and S. S. Kim, “26.5: Block-Wise Luminance Control Algorithm for AMOLED Image Sticking Mitigation,” SID Symp. Dig. Tech. Pap., vol. 42, no. 1, pp. 346–348 (2011).

[7] J. Rabaey, A. Chandrakasan, A. Nikolic, Digital Integrated Circuits: A Design Perspective, 2nd Edition, Prentice Hall (2003).