Electrical Characteristics of LTPS TFTs Fabricated by ELA with Laser Intensity Distributions Controlled by Dot Array Masks

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ABSTRACT

LTPS thin films are formed by using the ELA method, and it is known that the crystal grain size can be controlled by controlling the intensity distribution of the laser. In this study, we investigated the effect of intensity distribution during laser annealing on the electrical characteristics of LTPS TFTs.

1 Introduction

LTPS thin film transistors (TFTs) crystallized using the ELA method have high electron mobility and are therefore used as backplanes for active matrix organic displays [1]-[7].

However, it is difficult to increase the screen size because LTPS TFTs are formed on the glass substrate by scan irradiation of the line beam. The line beam scanning method is used when manufacturing a large display; therefore, the crystal grain size of the overlapping region becomes large owing to the folding of the beam, resulting in uneven device characteristics [8].

Previous studies focused on controlling the grain size by providing the laser with an intensity distribution and used a dot pattern mask to obtain the laser intensity distribution during annealing to control the grain size. Consequently, the change in the grain size in the folded region of the beam was reduced [9]. In this study, to clarify the optimum intensity distribution in this method, the size of the light-shielding area of the dot mask forming the intensity distribution was changed, and its relationship with the electrical characteristics was investigated.

2 Experiment

Fig. 1 is a schematic of the laser-annealing system used in this experiment. Annealing was performed using a KrF excimer-laser [GT600K/ Gigaphoton Inc., wavelength:248 nm, pulse duration (full width at half-maximum) of 82 ns with an intensity distribution to ensure a uniform grain size.

The dot mask was reduced and transferred using a 20 infinite-correction objective lens with a numerical aperture of 0.36, and the irradiation area was set to 200 μm × 200 μm. The fluence during laser annealing was 640–660 mJ / cm^2.

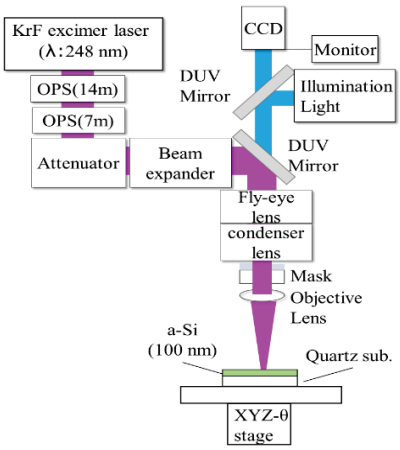

Fig. 1 Schematic of the excimer-laser annealing setup

2.1 Irradiation of Dot Mask Pattern Projection

Fig. 2 shows the LTPS crystallization state when a dot mask was used. The dot mask used was a synthetic quartz substrate, in which the dot-shaped Cr thin films were arranged at equal intervals. The intensity distribution of the laser beam was determined by the projection of the dot mask, and the beam intensity was low in the shielding area.

Therefore, when crystallization was performed after a-Si melting, crystal nuclei were generated in the region where the beam intensity was low and crystal growth was suppressed. Previous studies have used this method to form particles with sizes of 1.0-2.5 μm.

In this study, the dot pitch was set to 2 μm, and irradiation was performed using dot diameters of 0.25, 0.5, 1.0, 1.25, and 1.5 μm. Subsequently, the crystal state was observed and the electrical characteristics of the TFT were measured.

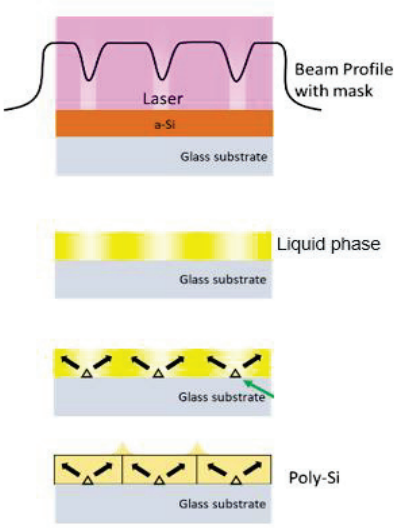

Fig. 3 Schematic of the crystallization process of poly-Si using ELA

2.2 TFT fabrication

An n-channel TFT was manufactured using the following process to evaluate the electrical characteristics of LTPS.

First, 100 nm of amorphous silicon was deposited on a synthetic quartz substrate at 550 °C by low-pressure chemical-vapor deposition (CVD). Next, amorphous silicon was crystallized into poly-Si by ELA. An island pattern was formed on the crystallized poly-Si thin film using photolithography, and etching was performed using a mixed solution of HF, HNO_3, and H_2O. SiO2 was deposited as a gate-insulating film using microwave-excited plasma-enhanced CVD at 100 nm. TiN was deposited on the gate electrode by reactive DC magnetron sputtering. A pattern was formed by photolithography, and then etching was performed with a mixed solution of HF, HNO_3, and H_2O. P + ions were injected into the channel region at 100 keV at a dose of $2 \times 10^{15} cm^{-2}$. Activation annealing was then performed at 550 °C for 1 h in N_2 atmosphere.

Next, SiO_2 was deposited as an interlayer insulating film at 400 °C at 150 nm by employing atmospheric-pressure CVD. Contact holes were formed by etching with an HF solution, Al was deposited by DC magnetron sputtering, and etching was performed with a mixed solution of H_3PO_4, CH_3COOH, HNO_3, and H_2O to form the source and drain electrodes. Finally, hydrogen annealing was conducted at 400 °C for 0.5 h. The length and width of the TFT channel produced in this study were 20 μm and 30 μm, respectively.

4 Result

Fig. 3 shows how the LTPS thin film after Secco etching was observed using a scanning electron microscope (SEM). The white dots in the grid position of the SEM images represent conical protrusions, and the black lines represent grain boundaries. These protrusions were formed at grain boundaries during the cooling process after laser annealing due to the difference in mass densities of the liquid phase and the solid phase silicon [10]. The LTPS thin film was formed using the dot mask, and these images show that square grains were formed at dot sizes of 0.5 – 1.5 μm, and radial grain boundaries [11] formed. Grain boundaries were present inside the square at a dot size of 1.25 and 1.5 μm. It was further observed that at a dot size 0.25 μm, the crystal grains varied.

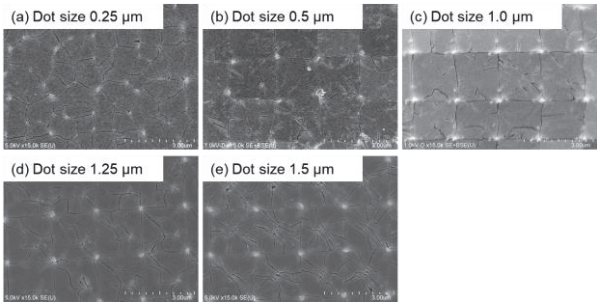

Fig. 3 (a)–(e) Scanning the electron microscopy images of each dot size in step-and-repeat annealing.

Table. 1 lists the results of measuring the field-effect mobility of TFT prepared for each dot size. At dot sizes of 0.5, 1.0, and 1.25 μm, the mobilities were 156 ± 15 cm^2 / Vs, 161 ± 20 cm^2 / Vs and 154 ± 20 cm^2 / Vs, respectively.

This was approximately 1.5 times as high as that of the conventional ELA method [12]. At a dot size of 0.25 and 1.5 μm, the mobility was 107 ± 22 cm^2 / Vs and 118 ± 21 cm^2 / Vs, respectively.

Table. 1 Experimental values of Electron mobility for each dot size in step-and-repeating

Dot size (μm)	0.25	0.5	1.0	1.25	1.5
μ_{FE} (cm^2/Vs)	107±22	156±15	161±20	154±20	118±21

Fig. 4 shows the dot size dependence of the field-effect mobility. The plots in Fig.4 show the field effect mobilities of each dot size.

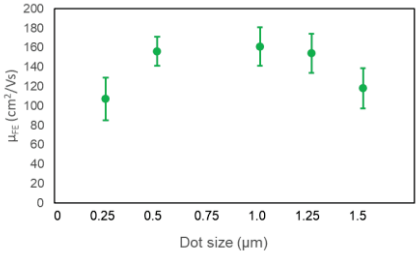

Fig. 4 Experimental result of field effect mobility of each dot size

5 Discussion

A likely reason for the mobility changes due to the difference in dot size is that there is a difference in the molten state of a-Si under the light-shielding region during laser annealing.

When the dot size was 0.5–1.25 μm, the laser intensity was sufficient to completely melt a-Si even in the light-shielded portion; thus, crystal nuclei were generated in the region where the laser intensity was low, and crystal growth occurred. Therefore, it is considered that square crystal grains corresponding to the dot pitch were formed, as shown in the SEM image, and high mobility was obtained.

When the dot size was 0.25 μm, the objective lens resolution was not sufficient (0.61 x λ / NA = 0.42 μm by Rayleigh's standard). Therefore, it is considered that the dots were not clearly projected, the intensity distribution was not sufficient to control the crystal nuclei, the crystal grains became non-uniform, and the mobility became almost the same as that of a general LTPS.

At a dot size of 1.5 μm, the light-shielding area was sufficiently large; therefore, the laser intensity of the light-shielding part was insufficient to completely melt a-Si, and many crystal nuclei were generated owing to the influence of unmelted a-Si. Therefore, it is probable that the mobility was low.

6 Conclusions

It was proven that the field-effect mobility of LTPS TFTs formed by excimer-laser annealing with intensity distribution changes depending on the size of the light-shielding region of the dot mask. Among them, the highest field-effect mobility at a dot size of 1.0 μm was 161 ± 20 cm^2 / Vs, which was approximately 1.5 times as high as that of the conventional ELA with a grain size of less than 350 nm.

References

[1] T. Sameshima, S. Usui, and M. Sekiya, “XeCl EXCIMER LASER ANNEALING USED IN THE FABRICATION OF POLY-Si TFT’S’.,” Electron device Lett., 1986, doi: 10.1109/edl.1986.26372.

[2] K. Shimizu, H. Hosoya, O. Sugiura, and M. Matsumura, “High-mobility bottom-gate thin-film transistors with laser-crystallized and hydrogen-radical-annealed polysilicon films,” Jpn. J. Appl. Phys., vol. 30, no. 12S, p. 3704, 1991.

[3] A. Hara, F. Takeuchi, and N. Sasaki, “Mobility enhancement limit of excimer-laser-crystallized polycrystalline silicon thin film transistors,” J. Appl. Phys., 2002, doi: 10.1063/1.1420766

[4] Y. Nakazaki et al., “Characterization of novel polycrystalline silicon thin-film transistors with long and narrow grains,” Japanese J. Appl. Physics, Part 1 Regul. Pap. Short Notes Rev. Pap., 2006, doi: 10.1143/JJAP.45.1489.

[5] M. Mitani, T. Endoy, S. Tsuboiz, T. Okaday, G. Kawachix, and M. Matsumura, “Relationship between thin-film transistor characteristics and crystallographic orientation in excimer-laser-processed pseudo-single-crystal- silicon films,” Jpn. J. Appl. Phys., 2010, doi: 10.1143/JJAP.49.124001.

[6] T. Goto et al., “LTPS Thin-Film Transistors Fabricated Using New Selective Laser Annealing System,” IEEE Trans. Electron Devices, 2018, doi: 10.1109/TED.2018.2846412.

[7] Flat Panel Display Manufacturing. 2018.

[8] Jin, G.H., Kim, M.: Characteristics of excimer laser-Annealed thin-film transistors on the polycrystalline silicon morphology formed in the single and double (overlap) scanned area. Jpn. J. Appl. Phys. (2010).

[9] Mizutani, A.; Hamano, F.; Nakamura, D.; Goto, T.; Aid, S. R. Size Effects of Poly-Si Formed by Laser Annealing with Periodic Intensity Distribution on the TFT Characteristics. IEEE J. Electron Devices Soc. 2021, 9, 679-686.

[10] B. W. Chen et al., “Surface Engineering of Polycrystalline Silicon for Long-Term Mechanical Stress Endurance Enhancement in Flexible Low-Temperature Poly-Si Thin-Film Transistors,” ACS Appl. Mater. Interfaces, 2017, doi: 10.1021/acsami.6b14525.

[11] D. Moschou, D. Kouvatsos, G. Kontogiannopoulos, F. Farmakis, and A. Voutsas, “Technology, performance and degradation characteristics of SLS ELA thin film transistors,” Facta Univ. - Ser. Electron. Energ., 2013, doi: 10.2298/fuee1303247m.

[12] M. Sobey, K. Schmidt, B. Turk, and R. Paetzel, “Status and future promise of Excimer Laser Annealing for LTPS on large glass substrates,” *Dig. Tech. Pap. - SID Int. Symp.*, 2014, doi: 10.1002/j.2168-0159.2014.tb00022.x.