## Cu Process Development of 43UD DRD TFT Architecture by Halftone Photolithography 4-Mask Technology

### <u>An-thung Cho</u>, Wei-wei Hu, Ren-hong Zhan, Wen-bing Wu, Ning-ning Li, Wanfei Yong, James Hsu, Wade Chen

david.cho@szhk.com.cn ChuZhou HKC Optoelectronics technology Co., Ltd., China Keywords: Cu process, Undercut, Passivation via hole, Interface, Pre-treatment

### ABSTRACT

Screen abnormality is a subject that needs to be overcome in the development of the TFT-LCD Cu process. Passivation undercut is one of the more difficult line defect problems to overcome because the ITO contacts M1 or M2 are discontinuous in the via hole causing screen anomalies. We describe in detail our approach to improve undercut of passivation via hole. The problem without any other side effects can be effectively solved by optimizing the film formation conditions and the pre-treatment before passivation layer deposition.

### 1. Introduction

Liquid crystal displays have been widely used in mobile phones, computers, televisions, automobile displays and other fields in recent years, and this phenomenon will last for a long time. Because of its low manufacturing cost and high yield, the Liquid crystal display using amorphous Si:H technology as TFT backplane is still the main product in the large size display field.[1,2,3] Passivation via hole plays a key role in contacting source/drain and pixel electrode in large size TFT-LCD production process. The size and profile of via hole have an important effect for improving the yield of the product. There have been some reports for improving via hole profile by tuning the dry etching process.[4] Herein, we improved via hole profile by optimizing the passivation layer's film forming conditions and the passivation layer's pre-treatment before deposition within the Cu-four-masks process TFT architecture on G8.6 substrate.

In general, the pixel electrode adopts ITO as the film layer, and the Source/Drain metal layer and pixel electrode contact via ITO. The most common defect of via hole is passivation layer undercut as shown in figure 1. When undercut happened, ITO break partly or wholly result in abnormal display. Passivation layer undercut was solved effectively by optimizing the passivation layer's film forming conditions and the passivation layer's pre-treatment before deposition without influence TFT character shown in this paper.

#### 2. Results and analysis

# 2.1 Improve via hole undercut by optimizing passivation layer's film formation conditions

ITO plays an important role of joint M1 and M2 through passivation via hole in GOA area. In addition, ITO fracture will lead to abnormal GOA signal and thus occurs gate side abnormal images. The yield loss of passivation undercut reaches 19.1%. Through analysis, we found that ITO had blast injury in abnormal area. There is high impedance due to thin ITO thickness at

some passivation undercut positions. When a high current passes through, it could cause a blast injury, and could occur gate side abnormal images in figure 2.

Before the deposition of the passivation layer, the channel of TFT and the surface of Source/Drain metal layer are exposed as described in figure 3. The plasma treatment before the deposition of the passivation layer will work on the surface both of the channel and Source/Drain metal layer. For the interface between the amorphous Si: H and passivation layer is important for leakage current of TFT which would result in image sticking of panels. So the followed different conditions for solving undercut must base on keeping no damages to the channel. Via hole profile was checked by scanning electron microscope (SEM). The electrical properties of TFT were test by Keysight E5270B instrument. Image sticking was test follow operating instructions.

Through a series of experiments, we found 25s heating combine 7s NH3 plasma with 8KW power before the deposition of passivation layer could gain good image sticking result. But the via hole exist undercut, and further experiments proved that longer NH3 plasma treatment time could improve undercut effectively with the image sticking getting worse (image sticking level the lower, the better) as shown in figure 4 and table 1. Obviously, the undercut and image sticking are trade off. One condition should be found to overcome both undercut and image sticking problem.

As the longer NH3 plasma treatment time, the better profile of via hole and the worse of image sticking. We considered that using another kind of gas to replace NH3 with keeping 7s NH3 plasma treatment invariability. We selected N2 to replace NH3 and set N2 plasma treatment time 10s, 15s and 20s with the power of 12KW as shown in table 2.

Final Result: As shown in figure 5, the SEM image of different conditions present via hole profile clearly. When N2 plasma was used before passivation layer deposition, undercut disappeared. We can find that all conditions used N2 plasma with 12KW power have satisfactory via hole profile. Further reliability testing indicated the image sticking of the three conditions keeping under L1 which meet specifications. More, we test the transfer characteristic curve of condition 1 and 6 as shown in figure 6. No significant differences were found from figure 6.

### 2.2 Cu Process TFT-LCD Fabrication

Figure 7 shows the display images of the 43DRD 60Hz TFT-LCD panel with Cu process using 4-mask a-Si TFT which was fabricated on HKC display's G8.6 (H2) LCD line.

### 3. Conclusions

We have successfully solved the passivation layer undercut issue by improve the adhesion of the interface between Source/Drain metal layer and passivation layer through tuning the pretreatment before passivation layer deposition. This kind of solution do not has great impact on the alteration of process and has no side effect appear of display.

### 4. Acknowledgements

This work was supported by HKC optoelectronics technology, China.

### 5. References

- [1] Kim, Da Eun, et al. "Corrosion Behavior and Metallization of Cu-Based Electrodes Using MoNi Alloy and Multilayer Structure for Back-Channel-Etched Oxide Thin-Film Transistor Circuit Integration." IEEE Transactions on Electron Devices 64.2(2017):447-454.
- [2] Yeon, Han Wool, et al. "Cu Diffusion Driven Dynamic Modulation of the Electrical Properties of Amorphous Oxide Semiconductors." Advanced Functional Materials 27.25(2017):1700336.
- [3] Cheng Wei Lin, Mo Hsun Tsai. "Etchant compositions and etching method for metals Cu/Mo." US patent No. 2010/0301010 AI.
- [4] Bo-Hyun Seo, Jae-Hong Jeon, Jorg Winkler et al. "A study on the galvanic reaction between Cu and Mo as well as MoW for TFT-LCD by using a zeroresistance ammeter." SID09 Digest, 1320-1323.



Figure 1. The schematic diagram of via hole and the phenomenon of undercut.



Figure 2. SEM/FIB analysis pictures of undercut



Figure 3. The schematic diagram of the plasma treatment before the deposition of the passivation layer

Condition	Heating	NH₃ plasma	Image sticking level
1	25s	7s, 8KW	LO
2	25s	10s, 8KW	L1
3	25s	15s, 8KW	L2
4	25s	20s, 8KW	L3

Table 1. Different pre-treatment condition before passivation layer deposition and corresponding image sticking level



Figure 4. The SEM image of via hole profile

Condition	Heating	NH₃ plasma	N <sub>2</sub> plasma
1	25s	7s, 8KW	0
5	25s	7s, 8KW	10s, 12KW
6	25s	7s, 8KW	15s, 12KW
7	25s	7s, 8KW	20s, 12KW

 Table 2. Different pre-treatment condition before

 passivation layer deposition





Figure 5. The SEM image of via hole profile.



Figure 6. The I-V curve of condition 1 and 6.



Figure 7. 43DRD 60Hz TFT-LCD panel with the Cu process using 4-mask a-Si TFT