Nanoscale Semiconductor Devices Fabricated using Adhesion Lithography at Low Cost

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ABSTRACT

As device features sizes decrease typically fabrication costs increase. By combining adhesion lithography, a fabrication technique to create nanodevices with bottom-up nanomaterial growth this manufacturing rule has been broken. Not only is the fabrication cheaper but there is a decrease in material wastage as compared to traditional top-down fabrication processes.

1 Introduction

Currently there is lots of interest in alternative techniques for nanofabrication of devices that are more cost effective than current industrial processes. Running concurrently to this is the desire to reduce the amount of wasted material seen in top-down fabrication [1].

Developed in 2014 Adhesion lithography (a-Lith) is a bottom-up technique that creates nanogaps (~10 nm) between different coplanar materials [1]. This small feature size is possible due to tuning of adhesion forces between different materials by using self-assembled monolayers. Much work has been carried on different applications with many different types of high-performance planar devices created [3-9]. These devices have been typically fabricated using thermal or electron beam evaporation which are not usually compatible with industrial process flows. Here we show an optimized process using sputtering to deposit nanogap electrodes. Graphene has then been deposited on top of the electrodes creating nano devices where the conduction of the graphene is greatly affected by being suspended over the nanogap devices.

2 Experiment

The devices were fabricated on Si wafers with 200 nm of SiO_2 as shown in Fig. 1. First 40 nm of Al was sputtered on to the wafers and patterned via a lift-off photolithography process using AZ5214E (Fig 1(a)). The sputtering system used is a high target utilization sputter (HiTUS) system (Plasm Quest Ltd.). Octadecylphosphonic acid (ODPA) in IPA (30mg:50ml) was then used to form a self-assembled monolayer (SAM) on the Al via dip coating for 20 mins (Fig 1 (b)). ODPA selectively attached to the Al and cause it to become more hydrophobic. A second

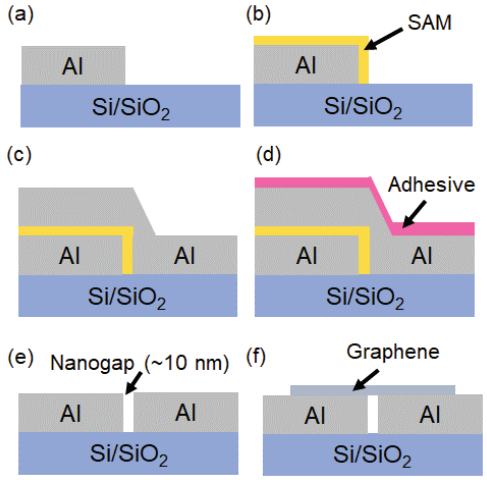

Fig. 1 Process for creating nanogap electrodes with graphene using adhesion lithography and a transfer of CVD grown graphene

layer of Al (40 nm thickness) was then sputtered on top of this (Fig. 1(c)), and an adhesive applied (First Contact adhesive from Photonic Cleaning Technologies) as shown in Fig. 1(d). As the adhesive was peeled off the substrate it removed the second layer of Al from on top of the first layer of Al but allowed it to remain on the substrate. This formed a nanogap (~10 nm) between the two metals, the SAM was then removed using a O_2 plasma. Fig 1(e) shows the resultant electrode structure. The Al was then patterned into final electrode shapes using photolithography and Al etchant. Graphene grown by chemical vapor deposition (CVD) as detailed in previous work was then transferred on top of the Al nanogap electrodes [10].

3 Results and Discussion

Using deposition processes that more readily allow for upscaling, like sputtering, means this process becomes more industrially viable. To be able to use sputtering successfully the choice of sputter system was very important. A critical process in the Adhesion lithography technique is the quality of the SAM layer, this needs to remain intact during the deposition of the second metal. With standard magnetron sputter coaters, typically

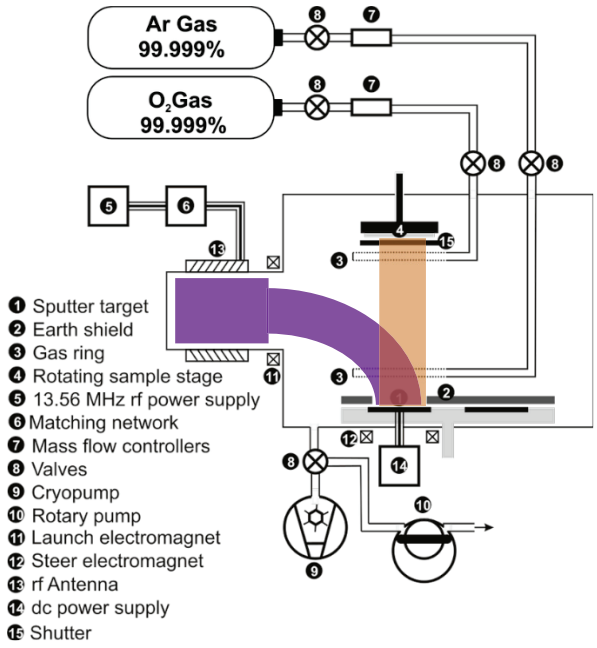

Fig. 2 High Target Utilization Sputter (HiTUS) system used to deposit metal electrodes (reproduced from [11]). It forms a remote plasma that is the directed to the target reducing ion bombardment on the sample

organic films can be damaged by ion bombardment. When standard sputtering has been attempted for the second Al layer the peel process has consistently failed due to damage of the SAM layer. In this work we used a sputter coater system called a HiTUS which due to its design is less damaging to organic layers during material deposition. The plasma is formed in a side chamber and then directed to the target so there is reduced ion bombardment on the samples (Fig. 2). This means that the SAM layer remains intact, and the second Al layer can be successful removed form on top of the first Al layer. It also utilizes more of the target material reducing issues with racetracks in the target material and has increased deposition rates.

The graphene growth process also used in this work has been optimized to be scalable. The Graphene layers are grown using a CVD process that is currently processed on 4" sized substrates but this is only limited by the size of the deposition chamber. The transfer process onto the a-Lith electrodes is also only limited by substrate size.

I-V measurements of the adhesion lithography electrodes are shown in Fig. 3. The empty nanogap shows electrical isolation between the two Al electrodes with a current of pA at the limit of the measurement system. For nanogap devices with the graphene placed across the gap, there is an increase in current that is dependent on channel width. For devices with a 2 mm channel the current increase to 0.1 nA for larger devices of 6 mm width the current increases further to 1 nA, showing a dependence of conductivity on device area. If these currents are compared to a larger scale device on the

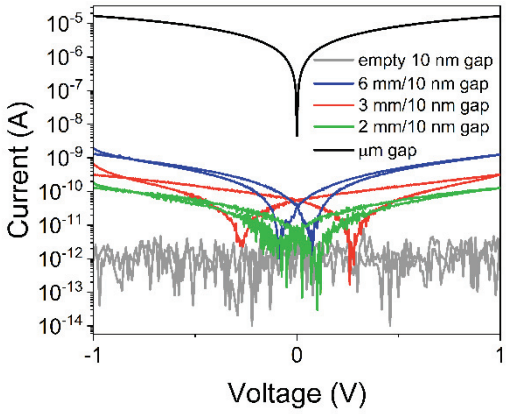

Fig. 3 I-V characteristics of nanogap electrodes with graphene

order of 100s µm the current is 10^4 lower in the nanogap devices (as shown in Fig. 3). This suggests that the nanogap devices are causing depletion of the graphene suspended over the gap reducing current flow. Three terminal measurements using the Si as a back gate have also been taken and will be discussed in more detail in the presentation.

4 Conclusions

In this paper we present results that show optimizing the processing of a-Lith we can get this high throughput technique towards industrial upscaling. By combining this process with a large area graphene growth and transfer process, we are able to create arrays of nanodevices.

5 Acknowledgements

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