Effect of Barrier Layer Properties of LTPS TFT Devices on AMOLED Short-term Image Sticking Performance

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ABSTRACT
As evidenced by our correlation analysis, reducing barrier layer roughness enhances AMOLED short-term image sticking performance. The results of microwave photoconductivity and interface trap density test demonstrated an reduced defect state density of polysilicon as the roughness of barrier layer decreased, leading to improved short-term image sticking performance.

1 Introduction
Much attention has been given to the short-term image sticking performance of AMOLED. Recent research has explored the link between short-term image sticking performance and the LTPS TFT device. This connection is primarily due to the changes in output current caused by electrical variations of driving TFT during screen switching. Thus, improving the performance of driving TFTs is crucial to enhance short-term image sticking performance[1].

Existing papers has shown that enhancing key layers characteristics, such as a-Si film, ELA crystallization, and gate insulator, can enhance LTPS device performance[2]. However, the mechanism of backside film layer on device characteristics and short-term image sticking are not fully understood. In order to investigate this, we made TFT device and panel samples, adjusting properties of barrier layer to examine the underlying relationship between them.

2 Experimental
In this study, we aimed to fabricate p-type channel LTPS TFT samples on polyimide substrate with top-gate structure. The experimental process involved depositing various properties of oxide barrier layer on polyimide substrate by plasma-enhanced chemical vapor deposition (PECVD). Additionally, a buffer layer oxide was deposited on top of the barrier layer. Afterward, a 50nm layer of amorphous silicon (a-Si) was deposited. The a-Si layer was then transformed into polycrystalline silicon through crystallization using a 308nm XeCl excimer laser annealing. A 120nm layer of silicon oxide was deposited as gate insulator, and a Mo gate pattern was applied as implant block layer. To form the ohmic contact area, high dose and energy of boron implantation were performed.

An interlayer dielectric was subsequently deposited using SiO₂. Source and drain electrodes were formed using TiAlTi. Based on these drive layer substrates, we made AMOLED panels to evaluate short-term image sticking properties.

To evaluate the performance of LTPS devices, I-V (current-voltage) and C-V (capacitance-voltage) characteristics are measured using Keithley 4200 instrument. μ-PCD(Microwave photoconductance Decay) test is used to evaluate crystalline quality of polycrystalline silicon.

3 Result and Discussion
3.1 Correlation between film properties of barrier layer and short-term image sticking
There are several potential reasons why the barrier layer may affect short-term image sticking performance. Firstly, changes in dielectric properties of barrier layer can alter electric field of LTPS TFT devices. Secondly, variations in barrier layer density can affect its ability to block substance diffusion under TFT device, leading to changes in electrical performance. Lastly, stress fluctuations within barrier layer can change stress distribution of whole device, particularly impact interface defect states and TFT device characteristics. However, our analysis of Fig. 2 revealed that the aforementioned conjectures are not significantly related to short-term image sticking performance. Instead, our findings suggest that the surface roughness of barrier layer is the key influencing factor.
Fig. 2 Correlation trend between LTPS TFT barrier layer properties and screen short-term image sticking performance (a) Relative Permittivity vs JNCD (Normalized). (b) Refractive Index vs JNCD (Normalized). (c) Film Stress vs JNCD (Normalized). (d) Surface Roughness Rq vs JNCD (Normalized)

3.2 Impact of barrier layer roughness on devices

To evaluate the impact of barrier layer roughness on TFT devices, we used microwave photocurrent method. However, accurate measurements are challenging due to defects in polycrystalline silicon. Sumie et al. [3] developed one test method by using microwave reflection signal’s amplitude voltage, which indirectly reflects the minority carrier lifetime of polycrystalline silicon. The amplitude of the signal is directly proportional to the minority carrier lifetime. Recombination centers, such as deep-level defects and tail-state defects, lead to minority carrier lifetime decrease. Therefore, a larger amplitude of microwave photocurrent reflection signal signifies superior crystalline quality in polycrystalline silicon, with fewer defects internally and on surface.

Analyzing the relationship between roughness of barrier layer and the amplitude of microwave photo current reflection signal in Fig. 3(a), it can be observed that the increase of barrier layer roughness leads to the polycrystalline silicon’s crystalline quality deterioration, and with that comes more defects. Consequently, this deterioration in TFT device characteristics can be observed. Specifically, for p-type LTPS (Low-Temperature Polycrystalline Silicon) TFT, the defects in active layer of polycrystalline silicon result in negative shift in the Vth (threshold voltage), along with SS increase (subthreshold slope). Fig. 3(b)

Table 1 AFM surface roughness Rq of buffer layer on different barrier layer surface roughness level

<table>
<thead>
<tr>
<th>Split</th>
<th>Barrier Layer Surface Roughness Rq(μm)</th>
<th>Buffer Layer Surface Roughness Rq(μm)</th>
<th>Buffer Layer Surface AFM Height Graphic</th>
</tr>
</thead>
<tbody>
<tr>
<td>Split1</td>
<td>0.99</td>
<td>1.67</td>
<td><img src="image1.png" alt="Image" /></td>
</tr>
<tr>
<td>Split2</td>
<td>2.05</td>
<td>3.05</td>
<td><img src="image2.png" alt="Image" /></td>
</tr>
<tr>
<td>Split3</td>
<td>4.44</td>
<td>7.02</td>
<td><img src="image3.png" alt="Image" /></td>
</tr>
</tbody>
</table>

3.3 Characteristic of LTPS TFT device

We fabricated TFT devices with different roughness levels at high, medium, and low conditions, with W/L=3μm/20μm. Fig. 5 shows the transfer characteristics curves of these devices under drain-source voltage of Vds = -0.1V. Table2 presents the results of the TFT device characteristics under three conditions.

From the results, it can be observed that as barrier layer roughness increases, the Vth of TFT devices shifts...
in a negative direction. Simultaneously, the SS increases accordingly. Additionally, the field-effect mobility decreases from 98.08 cm²/V·s to 90.41 cm²/V·s. These changes in device characteristics due to the increased presence of donor-type deep level defects in p-type LTPS TFTs are consistent with observed trends.

Based on the analysis of the data, we can infer the influence mechanism of the barrier layer's roughness on crystallization in the ELA process. The roughness of the barrier layer's surface leads to the formation of anomalous protrusions in a disordered manner. When subsequent CVD layers, such as the buffer layer, are applied, the roughness of the buffer layer's surface increases. Based on the crystallization principle of ELA[4], crystallization occurs when the material is almost completely melted. Initially, crystallization begins from the a-Si microcrystals on the buffer layer's surface. Therefore, the surface condition of the buffer layer significantly affects crystallization.

3.4 Polysilicon/Gate Insulator Interface Trap:
We measured the density distribution of defects at interface between polysilicon and gate insulator with respect to trap energy levels. We observed that Split3 defect density was the highest, followed by Split2, while Split1 had the lowest total defect density. This trend supports previous findings from μ-PCD and electrical characterization, providing additional confirmation of the relationship between barrier layer roughness and the occurrence of internal and interface defects in LTPS TFT devices.

The anomalous protrusions with unordered distribution on surface of buffer layer form points with higher surface energy. Crystallization nucleation will preferentially occur at positions with higher surface energy, which disrupts the uniformity of nucleation sites during initial crystallization of polycrystalline silicon. This leads to uneven grain size and chaotic crystalline growth, resulting in the formation of large number of grain boundaries and silicon-silicon weak bonds due to crystal-related defects. This, in turn, creates higher number of carrier defect sites.

3.5 Short-term image sticking performance:
The industry-standard method for testing short-term image sticking was used [5] (see Fig.8). The JNCD values were then calculated based on these brightness changes, providing an evaluation of short-term image retention severity according to equation (1) and equation (2), where $L(t)$ is the initial brightness of 48 Gray. $L(0)$ is display brightness at different times after switching black and white pattern to G48 pattern. $A$ and $B$ refers to different luminance test area.
Fig. 8 Schematic diagram of the short-term image sticking test process

\[ IS = \frac{L(t)_A - L(t)_B}{L(t)_A + L(t)_B} \]

\[ JNCD = \frac{IS}{0.004} \]

Analysis of JNCD values showed that increased roughness of barrier layer resulted in a significant deterioration of JNCD at 0 second. When roughness exceeded certain threshold (e.g., Split3), the JNCD values at 10 seconds significantly increase, indicating slower dissipation of image retention. This can be attributed to a higher concentration of deep-level trap in the Split3 PSi layer compared to Split2 and Split1. The large number of captured holes by deep-level defects results in slower emission process, leading to greater difference in TFT characteristics before and after grayscale switching, as well as slower recovery of TFT characteristics.

Fig. 9 Normalized JNCD data of display panels by adopting to different TFT fabrication processes of Split1-Split3

4 Conclusion

In this study, we investigated the relationship between the performance of barrier layer film and short-term image sticking in LTPS TFT. The results suggest that increase in roughness of barrier layer adversely affects the image sticking performance of display panel. We found that an increase in roughness of the underlying barrier layer lead to corresponding increase in roughness of upper buffer layer. Additionally, through \( \mu \)-PCD and interface trap density test, we confirmed that an increase in surface roughness of barrier layer resulted in polycrystalline silicon crystalline defects in the upper layer increase. These defects changed the characteristics of LTPS TFT devices and caused deterioration in the image sticking performance of the display. Following our findings, we proposed solution to improve short-term image sticking performance of AMOLED LTPS displays by reducing the barrier layer surface roughness. This improvement can be extended to all underlying layers of polycrystalline silicon, providing a key technological optimization direction for further enhancing the display’s short-term image sticking performance.

References


