An Empirical analysis on dimension dependent characteristics of low temperature Poly-Si Thin Film Transistors

MD Redowan Mahmud Arnob, Md. Hasnat Rabbi, Abul Tooshil, Sabiqun Nahar, Byeonggwan Kim and Jin Jang

jjang@khu.ac.kr
Department of Information Display, Advanced Display Research Center, Kyung Hee University, Seoul 02447, South Korea

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ABSTRACT
This research exemplifies the significance of grain boundary trap states in Blue Laser Annealed-Low temperature polysilicon (BLA-LTPS) Thin Film Transistors (TFTs) which yield the device dimension-dependent characteristics. The underlying mechanisms were analyzed by extracting grain boundary trap densities using Levinson’s plot.

1 Introduction
Instead of amorphous silicon, low-temperature polycrystalline silicon (LTPS) thin-film transistors (TFTs) have been employed as pixel and driving integrated circuits in active-matrix liquid crystal displays (AMLCDs) and active-matrix organic light-emitting diode displays (AMOLED) on glass and polyimide (PI) substrates [1-4]. Among several crystallization techniques, Blue Laser Annealing stands among one of the most prominent techniques that don’t or seldom concede the grain boundary protrusion effects due to its fully melted lateral crystallization [5-7]. However, the trap states in the grain boundaries might still cause device degradation, deteriorated uniformity, device instabilities, and lastly as discussed here dimension dependency [8-9].

Several researchers have worked on the dimension-dependent characteristics when scaling down channel length causes the contact resistance to increase which results in degradation of the field effect mobility but the exact role of grain boundary trap states remained unclarified [9].

In this work, self-aligned coplanar LTPS TFTs were fabricated via the BLA crystallization method on the glass substrate. Their dimension-dependent characteristics were analyzed by extracting grain boundary trap densities from Levinson Plot and compared based on different dimensions [10,11]. It was found that the downscaling of channel dimensions might lead to different trends in mobility due to the dominant characteristics of grain boundary trap states. Moreover, the grain size and TFT dimension ratio also play a major role in these different mobility trends.

2 Experiment
2.1 Device Fabrication
The cross-sectional view for the self-aligned top gate LTPS TFT on the glass substrate is demonstrated in Fig 1b. A 0.7T glass substrate, a 1000 nm SiO2 buffer layer was deposited by plasma-enhanced chemical vapor deposition (PECVD). Then, a 100 nm amorphous silicon layer was deposited using PECVD and dehydrogenated at 450°C for 4 hours under N2 conditions. Then, the crystallization procedure was undertaken using Blue Laser Annealing (BLA) with a laser power of 9.5 W as shown in Fig 1a. After the patterning of the active layer, a bilayer stacking of SiO2 (40 nm) and SiNx (70nm) was deposited as a Gate insulator (GI) by PECVD. As a gate electrode, 120 nm thick Mo was deposited via sputtering. For the self-aligned process, the GI and gate metal layers were etched before undertaking the P+ doping with B2H6 via Ion Implantation. An interlayer of 400 nm thick SiNx was deposited by PECVD followed by the deposition of 200 nm Mo, as the source/drain with via holes. Finally, a 400 nm SiO2 passivation was deployed.
2.2 Electrical Measurements

The electrical characterization was done in the dark at room temperature with an Agilent 4156C semiconductor device parameter analyzer. The threshold voltage \( V_{\text{th}} \) was considered to be the \( V_{\text{GS}} \) satisfying \( I_{\text{DS}}=W/L \times 10\text{pA} \) whereas the field effect mobility was determined from the transconductance parameter at \( V_{\text{DS}}=0.1\text{V} \). The subthreshold swing was taken as \((\text{dlog}(I_{\text{DS}})/\text{d}V_{\text{GS}})-1\) within a range of 10 pA<\( I_{\text{DS}} <100 \text{ pA} \), with \( V_{\text{DS}}=0.1 \text{V} \).

3 Results and Discussions

Fig 2a shows the length variation transfer curves at a constant \( V_{\text{GS}} \) sweeping range of +15 to -20 V at \( V_{\text{DS}}=-0.1\text{V} \) for all the TFTs considered here possess a dimension of \( W=20 \mu \text{m} \) with a length variation of 1.5, 2.0, 3.0, 5.0, and 10.0 \( \mu \text{m} \). As a channel length increases the \( I_{\text{on}} \) decreases as expected from the conventional current equation. The extracted threshold voltage, \( V_{\text{th}} \), and subthreshold swing, SS shows a mean value of -0.16 V and 0.141 respectively with a relatively small standard deviation of 0.114 in \( V_{\text{th}} \) and 0.007 in SS for all lengths. This shows the devices have less \( V_{\text{th}} \) or SS variation for increasing channel lengths. However, the field effect mobility, \( \mu_{\text{FE}} \) increases with the channel length as shown in Fig 1 and Table 1. Fig 2b shows the length variation (\( L=0.7, 1.0, 1.3, 1.5 \mu \text{m} \)) transfer characteristics of devices where the width is scaled down to \( W=1.5 \mu \text{m} \). These devices show less \( V_{\text{th}} \) and SS dependence on length too but a reverse trend in field effect mobility, \( \mu_{\text{FE}} \) as shown in Fig 2b and Table 2.

To investigate the reverse trend in mobility as a function of channel lengths for different widths, the grain boundary trap densities were extracted from the ln \( \left( I_{\text{DS}}/V_{\text{GS}} \right) \) vs \( 1/V_{\text{GS}} \) curve which is also known as Levinson’s Plot. Fig 3a shows the length variation summary of Levinson’s Plot for \( W=20 \mu \text{m} \) whereas Fig 3b shows the length variation summary of Levinson’s Plot when the width is scaled down to \( W=1.5 \mu \text{m} \). The grain boundary trap densities are relatively higher for devices having a smaller width which is also shown in Tables 1 and 2.

<table>
<thead>
<tr>
<th>Table 1 Length Variation parameter Summary for ( W=20 \mu \text{m} )</th>
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<tr>
<td>Length (( \mu \text{m} ))</td>
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<tr>
<td>1.5</td>
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<th>Table 2 Length Variation parameter Summary for ( W=1.5 \mu \text{m} )</th>
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<tr>
<td>Length (( \mu \text{m} ))</td>
</tr>
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</tr>
<tr>
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<tr>
<td>1.3</td>
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<td>1.5</td>
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Fig 4 Extraction of Channel resistance by TLM method from Total Resistance vs Channel length for different widths (a) \( W=20 \mu \text{m} \), (b) \( W=1.5 \mu \text{m} \), at \( V_{\text{DS}}=-0.1\text{V} \). Fig 4 shows the plot of Total Resistance vs Channel length, from which the channel resistances are predicted using the transmission line method (TLM). The devices with \( W=20 \) (Fig 4a) show a channel resistance of 1.02 KΩ/\( \mu \text{m} \) whereas the channel resistance increases to 22.94 KΩ/\( \mu \text{m} \) when the width is scaled down to \( W=1.5 \mu \text{m} \).
μm (Fig 4b). The greater channel resistance in W=1.5 μm devices can be attributed to the drop in mobility due to grain boundary trap states. The parasitic resistance in the contact regions is fairly low (1.66 KΩ) which also clarifies that the drop in mobility with the increased channel lengths is not due to the effects of parasitic resistances which are more dominant in short-channel as discussed by [9].

The bias stability analysis was conducted on those devices (W/L=1.5/0.7 μm), to investigate the short channel degradation. Fig 5 shows the evolution of transfer characteristics as a function of stress time up to 1 hour with V<sub>GS_stress</sub>= -20 V at a constant temperature of 60°C. With the negative bias temperature stress (NBTS) conducted on those devices, the ΔV<sub>th</sub> was found to be -0.4 V which can be attributed to the insignificant hole trapping in the ACT/GI interfaces leading to stable device performance.

Fig 5 Negative Bias Temperature stress at 60°C, Stress voltage of V<sub>DS</sub>= -20V, V<sub>GS</sub>=-0.1 V up to 1 hour for fabricated TFT having W/L=1.5/0.7μm

To clarify the underlying reasons for the different trends in mobility as a function of channel length the dimension and grain size ratios are necessary to be compared. The typical grain size of BLA-LTPS for such laser power tends to be less than 1μm as discussed by [5-7]. [9] also discussed the significance of grain boundary trap states to be more dominant if the grain sizes are almost similar to the dimension of fabricated TFTs. For W=20, the dimensions are quite large in comparison to the grain size and hence the grain boundary traps show less significance leading to an increase in mobility with channel length. The increase in mobility can be attributed to the longer diffusion lengths for the charge carriers who traverse through the channel with reduced scattering effects. In the case of the W=1.5 devices diffusion lengths are limited by the reduced dimension and hence more scattering which might be the reason for the drop in mobility. But the materialistic reasons for these different mobility trends are yet to be understood and remain a possible future study phenomenon to elucidate the transport mechanism of polycrystalline materials.

4 Conclusions

The dimension-dependent characteristics of BLA-LTPS thin film transistors were investigated focusing on the role of grain boundary trap states. The grain boundary trap densities were extracted using Levinson’s Plot and the values were compared according to the increment in channel length. The study revealed that when the active channel dimensions closely match the grain sizes, the influence of grain boundary trap states becomes more pronounced which might be the reason for the drop in mobility with channel length when the width is downscaled from 20 to 1.5 μm.

References


