C2RTL-Enabled Sustainable Computing: Building a RISC-V CPU Microdevice Platform for a Greener Future

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ABSTRACT
This paper introduces the possibility of utilizing C2RTL as an aid for the creation of a microdevice platform that would serve to reduce the amount of waste in both time and material. It also introduces an illumination sensor to be used as a sensor for the device.

1 Introduction
The pursuit of sustainable technology for IoT and Biomedical applications is crucial in the face of pressing environmental challenges. The exponential growth of computing systems necessitates eco-friendly innovations that minimize energy consumption and reduce electronic waste. Typically, in the fabrication of sensors, the circuit must also be designed to be able to convert the information from the sensor into a form that can be read by other circuits, usually in the form of an Analog-to-Digital Converter (ADC). The information from the ADC would then be usually processed further or simply transmitted to the wider network wirelessly through an RC circuit or other means of communication. While this analog design has often resulted in extremely small and efficient devices, in the case where there needs to be a change in the sensor device, either changing the sensor itself, a modification to the signal pattern or the communication method, the entire device would need to be thrown away even if the other parts of the device is still perfectly functional. Thus, we examine the usage of a lightweight CPU to be utilized as a platform that would bridge the sensors to the communication modules. Fig. 1 demonstrates how such a device might look.

Such a device is designed to be battery-less, harvesting the necessary energy needed for operation. Then under intermittent operation the CPU would in turn power the sensors and the communication module. As the CPU, sensors and the communication modules are separate it would be possible to simply change them as necessary. The programs inside the CPUs can also be changed. This ability to change the programs, sensors and communication module will greatly aid in mitigating the negative environmental impact associated with traditional computing systems.

However, the fabrication of a CPU necessitates the usage of digital design which currently in turn necessitates the usage of Verilog, a language that is specialized for the creation of circuits and FPGA programming but has little to no use outside of the aforementioned applications. As a result, not many are proficient in the language at least compared to other more commonly used languages such as C, C++ or python.

Traditional CPU architectures prioritize performance at the expense of energy efficiency, resulting in a significant carbon footprint. In this paper we utilize the open-source and energy-efficient RISC-V architecture that is renowned for its versatility, striking a balance between performance and sustainability.

2 Architecture
2.1 Microdevice Architecture
The overall architecture of the prototype can be seen below in Fig 2.

In this device, the sensor, an illumination sensing
circuit is connected to the Analog-to-Digital Converter (ADC) which is then connected to two mixed input and output (MIO) module, where one is utilized for control and other for information relay with the ADC and the RF circuit.

2.2 CPU Architecture

Fig. 3 CPU architecture detailing the main modules

The CPU architecture synthesized by C2RTL and modified in Verilog can be seen above in Fig 3. Two different MIO modules are used inside this device, MIO1 is utilized to accept information from the AD converter as well as transmit the processed information from the CPU to the transmitter. MIO2 is utilized for the control of the AD converter. A UART allows for the programming of the device with a baud rate of 152000 and which memory is being utilized can be controlled using the PAD.

2.3 Illumination Sensor

Utilizing the results from previous research we performed a linear regression to find the approximate amount of current that is generated per lux.

\[ Y = 0.53x + 4.0 \]

Then utilizing the information, we simulated the circuit seen below in Fig. 4. With the output PD being connected to a simulated photodiode.

Fig. 4 Schematic of the illumination sensor

The simulations utilize a bias voltage of 0.6V and an input voltage of 0.3V. The current passing through the photodiode is then varied from 0 to 1000 lux or a current of 0 to 538 nA. This range is chosen as it is this circuit is designed for indoor testing and 1000 lux appears to be the usual maximum amount of light for indoor use.

The voltage coming out of the OPAMP is then calculated to find the current across the resistance using the following formula.

\[ I_{PD} = \frac{V_{OUT} - V_{IN}}{R} \]

Then the resolution of the device per 0.29mV, the amount of voltage per ADC step.

3 Results & Discussion

3.1 CPU Layout

Fig. 5 Layout of the CPU and pins

The layout of the CPU sent for fabrication can be seen above in Fig. 5. The CPU itself measures approximately 1850x935 \( \mu \)m. While the resulting CPU is relatively large compared to previous versions reported by our laboratory [1], through further optimization of the code on both Verilog and the C2RTL, it is believed that the size can be further decreased. However, for this report we are focusing on the testing the practicality of the C2RTL thus other than adapting the C2RTL for fabrication as well as addition of a few modules, as little change is done to the CPU as possible. From the testing process it is noted that C2RTL’s main strength comes from its ability to easily add additional modules that are connected to the AXI-BUS. This means that the device can easily be expanded upon, as adding new modules such as MIOs can be done simply by duplicating lines of C++ code and assigning a new address to the new module. On the other hand, minor adjustments are still best-done using Verilog coding.

3.2 Illumination Sensor Layout

For the illumination sensor, a resistance of 240k\( \Omega \) is utilized resulting in a 2.25 lux per 0.29mV with a visual range from 0 to 6.52 \( \mu \)A or roughly 13,000 lux. While this range a lot larger than we needed, to lower the visual range we would need to increase the resistance exponentially to 2.7M\( \Omega \) resulting in a resolution of 0.19 lux per 0.29mV which is much finer than what is planned for this phase and would result in the resistance requiring a much larger amount of space. The larger range that is visible would also allow for limited testing of the device on the outside as well.
4 Conclusion

In conclusion, we have successfully synthesized a CPU utilizing code mainly from C2RTL. While there is more work to be done in regards to be done in both optimization and making the synthesized files ready to be used, we believe that what we introduced here today provides a good step forward for in the synthesis of an C2RTL-enabled microdevice.

We believe that the microdevice platform would serve as a gateway to allow for the reduction in the amount of time utilized and amount of materials wasted in the implementation of new devices both in testing and in production.

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