Development of the one-chip new type plasma wave spectrum receiver using the mixed-signal integrated circuit

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Plasma waves are the important observation target for scientific missions investigating space plasma phenomena, and many scientific satellites observe plasma waves using onboard plasma wave instruments. Plasma wave receivers are composed of electromagnetic sensors and a plasma wave receiver which processes signals picked up by sensors. The plasma wave receiver requires high-performance electronic circuits, and it causes an increase in mass and volume. On the other hand, the miniaturization of observation instruments is highly demanded. Part of its reasons is the expanding usage of microsatellites and the increasing onboard instruments of satellites.To resolve this problem, we use the Application-Specific Integrated Circuits (ASIC) technology which enables to miniaturize electronic circuits.

We propose new spectrum type receiver which combines analog circuits and digital signal processing. Conventional FFT-based receivers have the disadvantage in the difficulty of adjusting its receiver dynamic range to the dynamic range of target signals in a wide frequency range. The new receiver can overcome the disadvantage. The new receiver is composed of the analog part which applies band-limiting, amplifying, and anti-aliasing, the analog to digital converter (ADC), and the digital part which includes the FFT calculator and the controller of the receiver. The analog part has following three frequency band: band1: DC-1 kHz, band2: 1 kHz-10 kHz, band3: 10 kHz-100 kHz. The analog part changes the observation frequency band by altering the cutoff frequency of the band-limiting filter and the anti-aliasing filter via the external control signal. The controller sweeps observation band of the analog part, and we get the whole spectrum by applying FFT for waveforms in each band.

Our final goal is realizing the one-chip new spectrum receiver by developing all part of the receiver using ASIC. We already developed the analog part and the ADC by using ASIC. The dimension of the analog part is 4.21 mm x 1.16 mm and it of the ADC is 3.2 mm x 0.8 mm. To confirm the design of the digital part, we developed breadboard model of the receiver. The breadboard model is composed of the ASIC chip which includes the analog part and the ADC, and the FPGA which realizes digital part of the receiver. We confirmed that our design of the digital part can realize the new receiver. The breadboard model of the receiver has the time resolution of 112 msec, and its frequency resolution is 13 Hz in band1, 130 Hz in band2, and 1300 Hz in band3. We developed the ASIC chip which realizes the logic design confirmed by the breadboard model, and we will measure its performance.

In the presentation, we will show the detailed design and performance of the new spectrum receiver, especially we focus on the performance of the logic ASIC chip.

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