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Evaluation of Interface State Density of Strained-Si MOS Interfaces by Conductance Method

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Introduction Strained-Si (sSi) MOS devices have attracted considerable interests because of the high carrier mobility [1]. It has also been recently reported [2] that the introduced tensile strain can modify the properties of the SiO_2/sSi MOS interfaces. However, the nature of the generated interface defects and the physical origin for the robustness in sSi are still not clear.

On the other hand, the conductance method, proposed by Nicollian et al [3], has been widely used as one of the most accurate and informative methods for evaluating MOS interface states. However, to our best knowledge, there has not been yet any report on the application of the conductance method to the sSi MOS interfaces. In this paper, we report a novel approach to evaluate the properties of sSi MOS interface state by using the conductance method.

Experiments The structure of sSi MOS capacitors used in this experiment is shown in Fig.1. A 13-nm-thick biaxial tensile sSi layers were epitaxially grown on relaxed SiGe buffer layer on p-type Si substrates. The Ge content in the SiGe layers was 30%. The gate area of the MOS capacitors and the gate oxide thickness were 100μm x 100μm and 7.5nm, respectively. Interface states were introduced at SiO_2/Si and SiO_2/sSi interfaces by Fowler-Nordheim (FN) injection from the substrates with a constant gate current (30nA).

Results and discussion Fig. 2 show the conductance curves of the sSi MOS capacitors with the conventional equivalent circuit (Fig.3(a)) of conductance method. The unclear peak in the conductance curves suggests the influence of a serious series resistance effect, which is inherent to the sSi/SiGe MOS capacitors. The band offset for holes exist at the sSi/SiGe hetero-interface is known to provide a substantial amount of the resistance due to thermionic emission [4]. As a result, the appropriate subtraction of the series resistance is mandatory for successfully applying the conductance method to the sSi MOS capacitors. Based on the careful consideration of the hetero-interface, a novel correction method, called series resistance (G_s) and capacitance (C_s) correction method (SRCC), is employed to eliminate the parasitic effect due to the hetero-interface in the sSi MOS capacitors. Fig. 3(b) shows the equivalent circuit of SRCC. Here, C_s and G_s can be estimated from C-V and G-V in the accumulation region, as similar to the estimation of R_s in [3]. Fig. 4 shows the conductance curves of the sSi MOS capacitors after the SRCC. The clear peaks in the conductance curves, meaning that the present SRCC method can successfully eliminate the series admittance effect. Furthermore, in order to obtain the energy distribution of any parameters of interface defects, the position of surface potential ($E-E_v$) under a given gate voltage is needed. However, since the edge of the depletion layer in the sSi MOS capacitor with the very thin sSi layer locates in the SiGe buffer layer, conventional methods for Si MOS capacitors do not allow us to provide the position of surface potential. Thus, the position of surface potential is determined by using a device simulator, Sentaurus.

By employing the present evaluation method, we study the properties of interface states in sSi MOS capacitors generated by FN stress. Here, D_{it} is determined by the model including the surface potential fluctuation [3]. Fig. 5 shows the results of the SiO_2/sSi MOS interfaces in comparison with those of the SiO_2/Si ones. It is observed from Fig. 5 that the amount and the energy distribution of D_{it} at the SiO_2/sSi MOS interfaces are similar to those at the SiO_2/Si ones.

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References [1] S. Takagi et al, J. Appl. Phys., 80, 1567, 1996. [2] Y. Zhao et al, IEEE EDL, 32, 1005, 2011. [3] E. H. Nicollian and J. R. Brews, MOS Physics and Technology (Wiley, New York, 1982), Chap. 5. [4] S. Takagi et al., IEEE Trans. Electron Devices, 45, pp.494-501, 1998

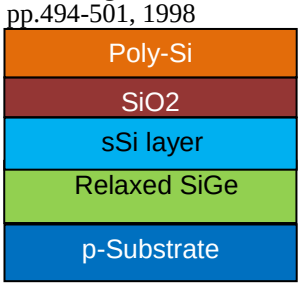

Fig. 1: The cross section of sSi capacitor

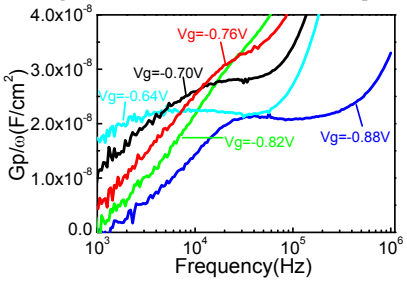

Fig. 2: Conductance curves of sSi capacitor without correction.

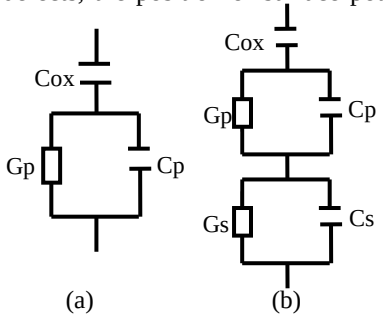

Fig. 3: (a) equivalent circuit of conventional conductance method (b) equivalent circuit of SRCC

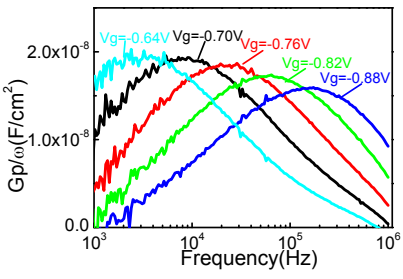

Fig. 4: Conductance curves of sSi capacitor with SRCC correction.

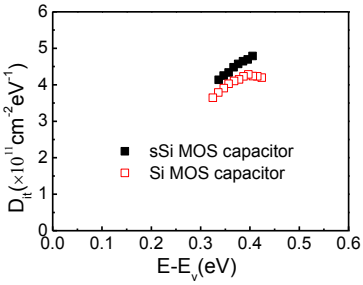

Fig. 5: D_{it} energy distribution of sSi/SiO2 and Si/SiO2 interfaces